Modeling the power-reliability tradeoff in on-chip networks

Claas Cornelius, Frank Sill, Dirk Timmermann

8th – 10th October 2007

12. Symposium Maritime Elektrotechnik, Elektronik und Informationstechnik

Rostock, 9th October 2007
12. Symposium Maritime Elektrotechnik, Elektronik und Informationstechnik
Outline

- Introduction
  - System design
  - Technology issues
- Approach
  - Analytical models
  - Simulation
- Results
- Summary
System design

Evolution

- Function-on-Chip
  - 1948 Shockley: Transistor
- Algorithm-on-Chip
  - 1958 Kilby: IC
- System-on-Chip
  - 1981 IBM: 5150 PC
- Network-on-Chip
  - ~2000: On-chip integration

Performance / Integration density
System design

Bus-based system design

- Shared communication medium

- Connected problems:
  - Memory-Bottleneck
  - Design-Productivity-Gap
  - Synchronous design

Chip-Area = 22 mm x 22 mm
System design

**Bus-based system design**

- Shared communication medium

- Connected problems:
  - Memory-Bottleneck
  - Design-Productivity-Gap
  - Synchronous design

- Worsening the situation:
  - Chip-Size
  - Interconnects
  - Integration density
  - Parameter variability
  - ... and many more

![Diagram of on-chip bus components]

- Chip-Area = 22 mm x 22 mm
System design

Wish list

Performance ↑
System complexity ↓
Power consumption ↓
Productivity ↑
Costs ↓

“... multi-core processors are another [...] 10x factor in terms of performance ...”

Paul Otellini, Intel President
IDF, September 2004

[Intel]
Network-on-Chip

Promising properties:
- Parallelism
- Modularity
Network-on-Chip

Promising properties:
- Parallelism
- Modularity

Level of abstraction:
- Modules
- Logic-Gates
- Transistors
- Polygons

Change of Paradigms:
- Computation
- Communication
Technology issues

Technology scenario 2010

- Technology node 45 nm
- Chip size 620 mm²
- Transistor count 4424 Mio.
- Physical gate length ~20 nm
- Metal layers 12-16
- Frequency (global-local) 2-12 GHz
- Total wire length ~2.2 km/cm²
  - For M1-M6, 33% usage

Approximate size of a resource
- Rent’s rule
- Reachable die area with clock signal
- Acceptable power trade-off

<10 Ångström gate oxide thickness
<100 dopant atoms

~85 resources
Power density

- Rocket nozzle
- Nuclear reactor
- Hot Plate
- 8008
- 8086
- 386
- P6
- Pentium® proc

Power Density (W/cm²)


[Borkar]
Technology issues

Parameter variability

<table>
<thead>
<tr>
<th>Parameter</th>
<th>250</th>
<th>180</th>
<th>130</th>
<th>90</th>
<th>65</th>
<th>45</th>
</tr>
</thead>
<tbody>
<tr>
<td>L (nm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vt (mV)</td>
<td>450</td>
<td>400</td>
<td>330</td>
<td>300</td>
<td>280</td>
<td>200</td>
</tr>
<tr>
<td>$\sigma$-Vt (mV)</td>
<td>21</td>
<td>23</td>
<td>27</td>
<td>28</td>
<td>30</td>
<td>32</td>
</tr>
<tr>
<td>$\sigma$-Vt/Vt</td>
<td>4.7%</td>
<td>5.8%</td>
<td>8.2%</td>
<td>9.3%</td>
<td>10.7%</td>
<td>16%</td>
</tr>
</tbody>
</table>

Normalized Leakage

Normalized Frequency

130nm ~1000 samples

30%

5x

Parameter variability dramatically increasing

[Devgan, 2003]

[ITRS, 2003]

[Borkar, 2005]
Approach

Related work

- Prototyping, Test-Chips
  - Star topology for multimedia applications [Lee, 2003]
  - 4x4 mesh network with traffic generators [Mullins, 2006]
- Parametrizable VHDL-model ported to FPGA [Zeferino, 2004]
- Emulation framework on an FPGA [Genko, 2005]
- High-level VHDL [Sigüenza, 2002]
- SystemC approach and design flow [Jalabert, 2004]
- Event-based C++ Simulator [Wiklund, 2004]
**Approach**

**Design space exploration**

1) Analytical models
   - Fast evaluation
   - Inaccurate Predictions

2) Simulation
   - Computation and time intensive
   - Accurate results
Analytical models

**Power equation**

\[
P_{\text{total}} = \alpha C_L V_{DD}^2 f + t_{SC} V_{DD} I_{\text{peak}} f + V_{DD} I_{\text{leakage}}
\]

- **Dynamic**
- **Short-Circuit**
- **Leakage**

E.g. Inverter

Output = Input

- Glitches, Spikes, Hazards:
  - Due to race conditions of signals
  - Hard to predict
  - Mostly empirical assessment
- Static power due to design style
Analytical models

Reliability

Process

Time

Environment

Random
Sytematic
Parametric

Within-die
Die-to-die
Wafer-to-Wafer

Device degradation
Electromigration
Mechanical stress
Thermal stress

Power supply
Ambient Temperature
Cooling

Crosstalk
EMI
α-particles

Electromigration
Mechanical stress
Thermal stress

Crosstalk
EMI
α-particles
Integration into a design flow

Simulator

Application specification (UML, C++ …)

Tasks, Stimuli

HWSW partitioning (Task mapping)

Resources (IPs)  Source (Processors)

NOC configuration

Topology, Traffic model etc.

NOC Simulator

NOC generation

RTL

Synthesis, Floorplan, Layout, Test …

NOC library
Simulation models
Implemented components

NOC Evaluator/Optimizer

Results (Visualization)
Results

Scenario

Simple example of 16 resources/IPs in a regular 4x4 mesh interconnected with

a) a Network-on-Chip

b) a single shared Bus
Results

Power and throughput

<table>
<thead>
<tr>
<th>Power consumption</th>
<th>Number of IPs (Total = N x N)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>4 9 16 25 36 49 64 81 100 121 144 169</td>
</tr>
<tr>
<td>Power</td>
<td>■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■</td>
</tr>
<tr>
<td>Power (with exploited locality)</td>
<td>▲ ▲ ▲ ▲ ▲ ▲ ▲ ▲ ▲ ▲ ▲ ▲ ▲ ▲ ▲ ▲ ▲</td>
</tr>
<tr>
<td>Power (with locality and DPM)</td>
<td>● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●</td>
</tr>
<tr>
<td>System throughput</td>
<td>□ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □</td>
</tr>
</tbody>
</table>

Claas Cornelius, October 2007
Institute of Applied Microelectronics and Computer Engineering, University of Rostock
Results

Power and throughput

- Power
- Power (with exploited locality)
- Power (with locality and DPM)
- System throughput

Power consumption vs. Number of IPs (Total = N x N)

- Graph showing trends in power consumption across different numbers of IPs.
- Bar chart illustrating system throughput.

Claas Cornelius, October 2007
Institute of Applied Microelectronics and Computer Engineering, University of Rostock
System control

Results

- Temperatur distribution influences
  - Performance
  - Power consumption
  - Reliability

- Dynamic power management
  - Avoid hot spots
  - Task mapping
  - Packet congestions
  - DV/FS, Clock-gating ...

Application example for the temperature distribution of a 5x5 network
Results

Reliability

- Permanent, single error
- Average number of working connections
- Cohesive connected system
Summary

- Motivation for investigating
  - Networks-on-Chip
  - Power and reliability
- Combined approach for design space exploration
- Comparison of results to a reference bus
- Consideration of dynamic behavior and control