Prof. Dr.-Ing. habil. Christian Haubelt

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Experience

06/2011- now	University of Rostock, Germany W3-Professor of Embedded Systems
10/2010-03/2011	University of Potsdam, Germany Substitute Professor of Computer Engineering
09/2008-10/2008:	UC Irvine, Center for Embedded Computer Systems, Irvine, CA, U.S.A. Visiting Researcher supported by Bavaria California Technology Center (BaCaTeC)
06/2005 – 05/2011	Institute Hardware-Software-Co-Design, Computer Science Department at the University of Erlangen-Nuremberg, Erlangen, Germany Habilitand (Researcher)
01/2004 – 05/2011	Head of the System-Level Design Automation (SDA) group at the Institute Hardware-Software-Co-Design, Computer Science Department at the University of Erlangen-Nuremberg, Erlangen, Germany
01/2003 - 05/2005	Institute Hardware-Software-C-Design, Computer Science Department at the University of Erlangen-Nuremberg, Erlangen, Germany Research Assistant
05/2001 - 12/2002	Computer Engineering Group; Electrical Engineering Department at the University of Paderborn, Paderborn, Germany Research Assistant

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Education

07/2010	University of Erlangen-Nuremberg, Erlangen, Germany Habilitation (postdoctoral lecture qualification) in Computer Engineering Thesis Title “Design and Verification of Embedded Digital Hardware/Software Systems”
06/2005	University of Erlangen-Nuremberg, Erlangen, Germany Dr.-Ing. (Ph.D.) in Computer Science, *summa cum laude* Thesis Title: „Automatic Model-Based Design Space Exploration for Embedded Systems – A System Level Approach“.
04/2001	University of Paderborn, Paderborn, Germany Diplom-Ingenieur (Diploma degree) in Electrical Engineering
07/1992	Herder Gymnasium, Minden, Germany Abitur (university entrance diploma)

Professional Services

Memberships:

1. IEEE (Institute of Electrical and Electronics Engineers, since 2001, Senior Member since 2014)
2. GI (Gesellschaft für Informatik, since 2009 member of the steering committee for the working group on "General Methodologies and Support of Circuit and System Design Processes")
3. HiPEAC (European Network of Excellence on High Performance and Embedded Architecture and Compilation, since 2012)
4. Wissenschaftsverbund IuK, (Wissenschaftsverbund "Entwicklung, Anwendung und Folgen moderner Informations- und Kommunikationstechnologien" der Universität Rostock, since 2012)

Editor:

1. SICS Software-Intensive Cyber-Physical Systems (since 2019)
2. Elsevier Journal of Systems Architecture, Subject Areas Editor “Multicore” und “Multiprocessor Systems” (2009 - 2014)

Reviewer:

Scientific organizations:

1. German Science Foundation (DFG)
2. Studienstiftung des deutschen Volkes
3. Technology Foundation STW, The Netherlands
4. The German Israeli Foundation for Scientific Research and Development

Textbooks:

5. Springer-Verlag Heidelberg/Berlin

Journals:

6. IEEE Transactions on Computers
7. IEEE Transactions on Computer Aided Design
8. IEEE Transactions on Parallel and Distributed Systems
9. IEEE Transactions on Very Large Scale Integration Systems
10. IEEE Transactions on Signal Processing
11. IEEE Transactions on Evolutionary Computation
12. IEEE Transactions on Multimedia
13. IEEE Embedded Systems Letters
14. IEEE Design & Test
15. ACM Transactions on Design Automation of Electronic Systems
16. ACM Transactions on Embedded Computer Systems
17. ACM Transactions on Reconfigurable Technology and Systems
18. Springer Journal on Design Automation for Embedded Systems
19. Springer Journal of Signal Processing Systems
20. Springer International Journal of Parallel Programming
21. Springer Computational Optimization and Applications
22. Sensors
23. Informatics
24. EURASIP Journal on Embedded Systems
25. Elsevier Microprocessors and Microsystems
26. Elsevier Journal of Systems Architecture
27. Elsevier Simulation Modelling Practice and Theory

Conference Organization:

1. Conference on Hardware/Software Codesign and System Synthesis 2016, 2017 (Track Chair "System-level design")
2. Design Automation and Test in Europe 2013-2016 (Topic Chair “System Specifications, Models and Methodologies”)
3. Conference on Hardware/Software Codesign and System Synthesis 2015 (Track Chair "Embedded systems architecture" and Best Paper Award committee member)
4. Electronic System Level Synthesis Conference 2014 (Program Chair)

5. Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen 2013 (Workshop Organizer)
6. Forum on Design Languages 2012 (Special Session Organizer “Invasive Programming of Heterogeneous Multi-Core Systems”)
7. Design Automation and Test in Europe 2012 (Friday Workshop Organizer “Quo Vadis, Virtual Platforms? - Challenges and Solutions for Today and Tomorrow”)
8. Conference on Systems, Architectures, Modeling, and Simulation 2011 (Special Session Organizer “What’s next in ESL”, pp. 330)
9. Conference on Systems, Architectures, Modeling, and Simulation 2010 (Topic Chair “Design Automation”)
10. Compiler-Assisted System-On-Chip Assembly 2010 (Workshop Organizer)
11. Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen 2007 (Workshop Organizer)

Program Committee:

1. Conference on Hardware/Software Codesign and System Synthesis 2007 – 2020
2. Workshop on Software and Compilers for Embedded Systems 2012 – 2014, 2016 – 2020
3. Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools 2016 – 2020
4. Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen 2007 – 2020
5. Conference on Systems, Architectures, Modeling, and Simulation 2010 – 2019
6. Forum on Design Languages 2006 – 2019
7. International Conference on Language, Compilers, Tools and Theory of Embedded Systems 2019
8. Design Automation and Test in Europe 2008 – 2016
9. International Workshop on Multi-Objective Many-Core Design 2014 – 2016
10. Workshop on Integrating Dataflow, Embedded computing and Architecture 2016
11. Design Automation Conference 2015
12. Electronic System Level Synthesis Conference 2011 – 2015
13. Asia and South Pacific Design Automation Conference 2014
14. International Conference on Embedded and Ubiquitous Computing 2014
15. International Conference on Computer-Aided Design 2011 – 2013
16. Real-Time and Embedded Technology and Applications Symposium 2013
17. Reconfigurable Architectures Workshop 2012
18. Workshop on Cyber-Physical Systems 2011, 2012
19. Conference on Evolutionary Multi-Criterion Optimization 2007 – 2011
20. Congress on Evolutionary Computation 2005 - 2010
21. Workshop on Systems, Architectures, Modeling, and Simulation 2009
22. Conference on Computational Intelligence and Security 2007, 2008
23. Genetic and Evolutionary Computation Conference 2006

Publications

Books:

1. C. Haubelt and D. Timmermann. *Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen*. Rostock, Germany, 2013.
2. C. Haubelt and J. Teich. *Digitale Hardware/Software-Systeme: Spezifikation und Verifikation*. Springer-Verlag, Berlin Heidelberg, 2010.
3. J. Teich and C. Haubelt. *Digitale Hardware/Software-Systeme: Synthese und Optimierung*. 2. Auflage, Springer-Verlag, Berlin Heidelberg, 2007.

4. C. Haubelt and J. Teich. *Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen*. Shaker Verlag, Aachen, Germany, 2007.
5. C. Haubelt. *Automatic Model-Based Design Space Exploration for Embedded Systems - A System Level Approach*. Dissertation, University of Erlangen-Nuremberg, ISBN 3-89574-572-3, © Verlag Dr. Köster, Berlin, 2005.

Book Chapters:

1. J. Falk, K. Neubauer, C. Haubelt, C. Zebelein, and J. Teich. *Integrated Modeling Using Finite State Machines and Dataflow Graphs*. In Handbook of Signal Processing Systems, 3rd ed., pp. 825 – 864, Springer, 2019.
2. J. Falk, C. Haubelt, J. Teich, and C. Zebelein. *SysteMoC: A Dataflow Programming Model for Codesign*, In Handbook of Hardware/Software Co-Design, pp. 1-39, Springer, 2017.
3. S Ha, J. Teich, C. Haubelt, M. Glaß, T. Mitra, R. Dömer, P. Eles, A. Shrivastava, A. Gerstlauer, and S. S. Bhattacharyya. *Introduction to Hardware/Software Co-Design. In Handbook of Hardware/Software Co-Design*, pp. 1-24, Springer, 2017.
4. J. Falk, C. Haubelt, C. Zebelein, and J. Teich. *Integrated Modeling Using Finite State Machines and Dataflow Graphs*. In Handbook of Signal Processing Systems, 2nd ed., pp. 975-1013, Springer, 2013.
5. M. Streubühr, J. Gladigau, C. Haubelt and J. Teich. *Efficient Approximately-Timed Performance Modeling for Architectural Exploration of MPSoCs*. In Advances in Design Methods from Modeling Languages for Embedded Systems and SoC's, pp. 59-72, Springer, 2010.
6. J. Falk, J. Keinert, C. Haubelt, J. Teich and C. Zebelein. *Integrated Modeling Using Finite State Machines and Dataflow Graphs*. In Handbook of Signal Processing Systems, pages 1041-1075, Springer, 2010.
7. C. Haubelt, D. Koch, F. Reimann, T. Streichert and J. Teich. ReCoNets – Design Methodology for Embedded Systems Consisting of Small Networks of Reconfigurable Nodes and Connections. In Dynamically Reconfigurable Systems - Architectures, Design Methods and Applications, pages 223-244. Springer, Heidelberg, 2010.
8. J. Gladigau, C. Haubelt and J. Teich. *Symbolic Scheduling of SystemC Dataflow Designs*. In M. Radetzki, editor, Languages for Embedded Systems and their Applications, volume 36 of Lecture Notes in Electrical Engineering, pages 183–199. Springer Netherlands, 2009.
9. T. Streichert, C. Haubelt, D. Koch and J. Teich. *Concepts for Self-Adaptive and Self-Healing Networked Embedded Systems*. Organic Computing, Rolf Würtz (Ed.), Springer Series Understanding Complex Systems, pp. 241-260, Springer, 2008.
10. B. Niemann, C. Haubelt, M. Uribe and J. Teich. *Formalizing TLM with Communicating State Machines*. In Advances in Design and Specification Languages for Embedded Systems, pp. 225-242, Springer, 2007.
11. C. Haubelt, S. Mostaghim, F. Slomka, J. Teich and A. Tyagi. *Hierachical Synthesis of Embedded Systems Using Evolutionary Algorithms*. In Evolutionary Algorithms in System Design by Drechsler, R. and Drechsler, N., in Genetic Algorithms and Evolutionary Computation (GENA), pp. 63-104, Kluwer Academic Publishers, Boston, Dordrecht, London, 2003.
12. C. Haubelt, J. Teich, K. Richter and R. Ernst. *Flexibility / Cost-Tradeoffs of Platform-Based Systems*. In Embedded Processor Design Challenges, E. Deprettere, J. Teich, and S. Vassiliadis, editors, Lecture Notes in Computer Science (LNCS), Vol. 2268, pp. 38-56, Springer, Berlin, Germany, March 2002.

Reviewed Journal Articles:

1. F. Hölzke, J.-P. Wolff, F. Golatowski, and C. Haubelt. *Low-Complexity Online Correction and Calibration of Pedestrian Dead Reckoning Using Map Matching and GPS.* In Journal Geo-Spatial Information, pp. 1-14, Mai 2019
2. F. Grützmacher, A. Hein, T. Kirste, and C. Haubelt. *Model-Based Design of Energy Efficient Human Activity Recognition Systems with Wearable Sensors*. Technologies 6(4), 89:1 – 89:20, 2018.
3. M. Rethfeldt, B. Beichler, P. Danielis, F. Uster, C. Haubelt, and D. Timmermann. *MeNTor: A Wireless-Mesh-Network-Aware Data Dissemination Overlay based on BitTorrent*. Elsevier Ad Hoc Networks, Volume 79, pp. 146-159, Elsevier B. V., Amsterdam, The Netherlands, Oktober 2018

4. F. Grützmacher, B. Beichler, A. Hein, T. Kirste, and C. Haubelt. *Time and Memory Efficient Online Piecewise Linear Approximation of Sensor Signals*. Sensors 18(6), pp. 1672:1 – 1672:20, 2018.
5. C. Haubelt, K. Neubauer, T. Schaub, and P. Wanko. *Design Space Exploration with Answer Set Programming.* In KI - Künstliche Intelligenz, pp. 1 – 2, 2018.
6. S. Stieber, R. Dorsch, and C. Haubelt. *Accurate Sample Time Reconstruction of Inertial FIFO Data*. Sensors 17(12), pp. 2894:1 – 2894:15, 2017.
7. M. Geilen, J. Falk, C. Haubelt, T. Basten, B. Theelen, and S. Stuijk. *Performance Analysis of Weakly-Consistent Scenario-Aware Dataflow Graphs*. The Journal of Signal Processing Systems 87(1). pp. 157-175, 2017.
8. L. Middendorf and C. Haubelt. *A Programmable Graphics Processor based on Partial Stream Rewriting*. In Computer Graphics Forum 32(7), pp. 325-334, 2013.
9. J. Falk, C. Zebelein, C. Haubelt, and J. Teich. *A Rule-Based Quasi-Static Scheduling Approach for Static Islands in Dynamic Dataflow Graphs*. ACM Transactions on Embedded Computing Systems 12(3), pp. 74:1 – 74:31, 2013.
10. J. Gladigau, C. Haubelt, and J. Teich. *Model-Based Virtual Prototype Acceleration*. In IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 31(10), pp. 1572 – 1585, 2012.
11. R. Dorsch, R. K. Errickson, M. M. Helms, G. Crew, T. A. Gregg, W. Haileselassie, L. W. Helmer, A. Kohler, K. M. Pandey, S. Roscher, E. S. Rotter, C. Haubelt. *IBM Parallel Sysplex design for the IBM z196 system*. IBM Journal of Research and Development 56(1): 9, 2012.
12. J. Gladigau, A. Gerstlauer, C. Haubelt, M. Streubühr, and J. Teich. *Automatic System-Level Synthesis: From Formal Application Models to Generic Bus-Based MPSoCs.* In Transactions on HiPEAC 5(4), pp. 1-22, 2011.
13. J. Falk, C. Zebelein, J. Keinert, C. Haubelt, J. Teich and S. S. Bhattacharyya. *Analysis of SystemC Actor Networks for Efficient Synthesis*. In ACM Transactions on Embedded Computing Systems, 10(2):94–127, 2010.
14. A. Gerstlauer, C. Haubelt, A. D. Pimentel, T. P. Stefanov, D. D. Gajski and J. Teich. *Electronic System-Level Synthesis Methodologies*. In IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 28(10), pp. 1517-1530, 2009.
15. J. Keinert, M. Streubühr, T. Schlichter, J. Falk, J. Gladigau, C. Haubelt, J. Teich and M. Meredith. *SYSTEMCODESIGNER - An Automatic ESL Synthesis Approach by Design Space Exploration and Behavioral Synthesis for Streaming Applications*. In ACM Transactions on Design Automation of Electronic Systems, 14(1), pp. 1-23, 2009.
16. T. Streichert, M. Glaß, C. Haubelt and J. Teich. *Design Space Exploration of Reliable Networked Embedded Systems*. In Journal on Systems Architecture (JSA). Volume 53(10): 751-763, 2007.
17. F. Dittmann, F. Rammig, M. Streubühr, C. Haubelt, A. Schallenberg and W. Nebel. *Exploration, Partitioning and Simulation of Reconfigurable Systems*. it - Information Technology, http://it-information-technology.de , Oldenbourg Wissenschaftsverlag, vol. 49(3):149-156, 2007.
18. T. Streichert, C. Strengert, D. Koch, C. Haubelt and J. Teich. *Communication Aware Optimization of the Task Binding in Hardware/Software Reconfigurable Networks*. Journal on Integrated Circuits and Systems, Volume 2, Number 1, pp. 29-36, March 2007.
19. C. Haubelt, J. Falk, J. Keinert, T. Schlichter, M. Streubühr, A. Deyhle, A. Hadert and J. Teich. *A SystemC-based Design Methodology for Digital Signal Processing Systems*. In EURASIP Journal on Embedded Systems, Special Issue on Embedded Digital Signal Processing Systems, Volume 2007 (2007), Article ID 47580, 22 pages, March 2007.
20. T. Streichert, D. Koch, C. Haubelt and J. Teich. *Modeling and Design of Fault-Tolerant and Self-Adaptive Reconfigurable Networked Embedded Systems*. EURASIP Journal on Embedded Systems, Volume 2006 (2006), Article ID 42168, 15 pages, Hindawi Publishing Corporation.
21. C. Haubelt, T. Schlichter and J. Teich. *Improving Automatic Design Space Exploration by Integrating Symbolic Techniques into Multi-Objective Evolutionary Algorithms*. In International Journal of Computational Intelligence Research (IJCIR), Special Issue on Multiobjective Optimization and Applications, Volume 2, Issue 3. pp. 239-254, 2006.

Patents:

1. A. Biewer, J. Gladigau, C. Haubelt, and D. Thoss. *Controlling Device for an Automobile*. TW00000I651652B, Taiwan Patent, Feb. 21, 2019.
2. R. Dorsch, C. Haubelt, S. Liu, and S. Stieber. *Method for Adjusting Time Stamps During the Acquisition of Sensor Data*. China Patent Application CN000109286461A, Jan. 29, 2019.

3. R. Dorsch, C. Haubelt, S. Liu, and S. Stieber. *Method for Adjusting Time Stamps During the Acquisition of Sensor Data*. US Patent Application US020190028261A1, Jan. 24, 2019.
4. R. Dorsch, C. Haubelt, S. Liu, and S. Stieber. *Verfahren zum Anpassen von Zeitstempeln bei der Erfassung von Sensordaten*. Offenlegungsschrift DE102017212353A1, Jan. 24, 2019.
5. R. Dorsch, C. Haubelt, L. Middendorf, and S. Stieber. Processing Control of a Sensor System. Taiwan Patent Application TW000201839606A, Nov. 1, 2018.
6. R. Dorsch, C. Haubelt, L. Middendorf, and S. Stieber. *Verarbeitungssteuerung eines Sensorsystems*. Offenlegungsschrift DE102017204514A1, Sep. 20, 2018.
7. R. Dorsch, C. Haubelt, L. Middendorf, and S. Stieber. Processing Controller of a Sensor System. WIPO Patent Application WO2018/166698A1, Sep. 20, 2018.
8. A. Biewer, J. Gladigau, C. Haubelt, and D. Thoss. *Control Device for a Motor Vehicle*. European Patent EP000003077912B1, Aug. 08, 2018.
9. R. Dorsch, C. Haubelt, S. Stieber, and A. C. Strohrmann. *Methods for Detecting a Double-Click Input*. United States Patent US 10,031,611 B2, Jul. 24, 2018.
10. D. Koch, T. Streichert, C. Haubelt and J. Teich. *Logic Chip, Logic System and Method for Designing a Logic Chip*. EP2188894B1, October 18, 2017.
11. A. Biewer, J. Gladigau, C. Haubelt, and D. Thoss. *Control Device for a Motor Vehicle*. US Patent Application US020160299839A1, Oct. 13, 2016.
12. A. Biewer, J. Gladigau, C. Haubelt, and D. Thoss. *Control Device for a Motor Vehicle*. European Patent Application EP000003077912A1, Oct. 12, 2016.
13. A. Biewer, J. Gladigau, C. Haubelt, and D. Thoss. *Control Device for a Motor Vehicle*. South Korea Patent Application KR102016093621A, Aug. 08, 2016.
14. A. Biewer, J. Gladigau, C. Haubelt, and D. Thoss. *Control Device for a Motor Vehicle*. China Patent Application CN000105765541A, Jul. 13, 2016.
15. A. C. Strohrmann, C. Haubelt, R. Dorsch, and S. Stieber. *Methods for Detecting a Double-Click Input*. China Patent Application CN000105739755A, Jul. 06, 2016.
16. R. Bichler, T. Claus, R. Dorsch. C. Haubelt, and L. Middendorf. *Apparatus and Method for Calibration and Self-Test of Inertial Sensors*. South Korea Patent Application KR102016072055A, Jun. 22, 2016.
17. R. Bichler, T. Claus, R. Dorsch. C. Haubelt, and L. Middendorf. *Device for Adjusting and Self-Testing Inertial Sensors, and Method*. China Patent Application CN000105699696A, Jun. 22, 2016.
18. R. Bichler, T. Claus, R. Dorsch. C. Haubelt, and L. Middendorf. *Device for Adjusting and Self-Testing Inertial Sensors, and Method*. US Patent Application US020160170502A1, Jun. 16, 2016.
19. R. Dorsch, C. Haubelt, A. C. Strohrmann, and S. Stieber. *Verfahren zur Erkennung einer Doppelklickeingabe*. Offenlegungsschrift DE102014225853A1, Jun. 16, 2016.
20. R. Bichler, T. Claus, R. Dorsch, C. Haubelt, and L. Middendorf. *Vorrichtung zum Abgleich und Selbsttest von Inertialsensoren und Verfahren*. Offenlegungsschrift DE102015203968A1, Jun. 16, 2016.
21. R. Dorsch, C. Haubelt, S. Stieber, and A. C. Strohrmann. *Methods for Detecting a Double-Click Input*. US Patent Application US020160170557A1, Jun. 16, 2016.
22. A. Biewer, J. Gladigau, C. Haubelt, and D. Thoss. *Controling Device for an Automobile*. Taiwan Patent Application TW000201533665A, Sep. 01, 2015.
23. A. Biewer, D. Thoss, J. Gladigau, and C. Haubelt. *Control Device for a Motor Vehicle*. WIPO Patent Application WO2015/082109A1, Jun. 11, 2015.
24. A. Biewer, D. Thoss, J. Gladigau, and C. Haubelt. *Steuergerät für ein Kraftfahrzeug*. Offenlegungsschrift DE102013224702A1, Jun. 3, 2015.
25. D. Koch, T. Streichert, C. Haubelt and J. Teich. *Logic Chip, Method and Computer Program for Providing a Configuration Information for a Configurable Logic Chip*. United States Patent 8,554,972 B2, Oct. 8, 2013.
26. D. Koch, T. Streichert, C. Haubelt and J. Teich. *Logic Chip, Logic System and Method for Designing a Logic Chip*. United States Patent 8,018,249 B2, Sep. 13, 2011.
27. D. Koch, T. Streichert, C. Haubelt and J. Teich. *Logic Chip, Method and Computer Program for Providing a Configuration Information for a Configurable Logic Chip*. Patent Application Publication US 2011/0055449 A1, Mar. 3, 2011.
28. D. Koch, T. Streichert, C. Haubelt and J. Teich. *Logic Chip, Logic System and Method for Designing a Logic Chip*. Patent Application Publication US 2010/0283505 A1, Nov. 11, 2010.
29. D. Koch, T. Streichert, C. Haubelt and J. Teich. *Logic Chip, Logic System and Method for Designing a Logic Chip*. Patent Application EP2188894A1, May 26, 2010.

30. D. Koch, T. Streichert, C. Haubelt and J. Teich. *Logic Chip, Method and Computer Program for Providing a Configuration Information for a Configurable Logic Chip*. Patent Application EP2188735A1, May 26, 2010.
31. D. Koch, T. Streichert, C. Haubelt and J. Teich. *Logic Chip, Logic System and Method for Designing a Logic Chip*. WIPO Patent Application WO/2009/033630 A1, Mar. 19, 2009.
32. D. Koch, T. Streichert, C. Haubelt and J. Teich. *Logic Chip, Method and Computer Program for Providing a Configuration Information for a Configurable Logic Chip*. WIPO Patent Application WO/2009/033631 A1, Mar. 19, 2009.

Reviewed Conference Papers:

1. F. Grützmacher, B. Beichler, C. Haubelt. *Model-Based Real Time Analysis of Distributed Human Activity Recognition Stages in Wireless Sensor Networks.* In Adjunct Proceedings of the 2019 ACM International Joint Conference on Pervasive and Ubiquitous Computing and the 2019 International Symposium on Wearable Computers (UbiComp/ISWC '19 Adjunct), pp. 73-76, London, England, September 2019.
2. A. Wellnitz, J.-P. Wolff, C. Haubelt, T. Kirste, and S. Bader. *Fluid Intake Recognition using Inertial Sensors*. In Proceedings of the International Workshop on Sensor-based Activity Recognition and Interaction (iWoAR'19), Rostock, Germany, September, 2019. (to appear)
3. N. Büscher, D. Gis, S. Stieber and C. Haubelt. *Multi-Aspect Evaluation Method for Digital Pointing Devices*. In Proceedings of Pervasive and Embedded Computing and Communication Systems (PECCS'19), pp. 128-135, Vienna, Austria, September 2019.
4. J. Rudolf, D. Gis, S. Stieber, C. Haubelt, and R. Dorsch: *SystemC Power Profiling for IoT Device Firmware using Runtime Configurable Models*. In Proceedings of the Mediterranean Conference on Embedded Computing (MECO'2019), pp. 1-6, Budva, Montenegro, June, 2019.
5. J. Rudolf, M. Strobel, J.-J. Benz, C. Haubelt, M. Radetzki, and O. Bringmann. *Automated Sensor Firmware Development - Generation, Optimization, and Analysis*. In Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV19), pp. 60-71, Kaiserslautern, Germany, April 2019.
6. F. Hölzke, J.-P. Wolff, and C. Haubelt. *Improving Pedestrian Dead Reckoning using Likely Paths and Backtracking*. In IEEE International Conference on Pervasive Computing and Communications Workshops (PerCom Workshops), pp. 1-4, Kyoto, Japan, March 2019.
7. M. Rethfeldt, B. Beichler, P. Danielis, T. Brockmann, C. Haubelt, and D. Timmermann. *CHaChA: Clustering Heuristic and Channel Assignment for IEEE 802.11s Mesh Networks*. In Proceedings of the 9th IEEE Annual Information Technology, Electronics & Mobile Communication Conference (IEMCON), pp. 461-467, Vancouver, Kanada, November 2018.
8. K. Neubauer, P. Wanko, T. Schaub, and C. Haubelt. *On Leveraging Approximations for Exact System-level Design Space Exploration*. In Proceedings International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), pp. 15, Torino, Italy, October, 2018.
9. J.-P. Wolff, F. Grützmacher, A. Wellnitz and C. Haubelt, *Activity Recognition using Head Worn Inertial Sensors*, In Proceedings of the 5th international Workshop on Sensor-based Activity Recognition and Interaction, 14:1 – 14:7, Berlin, Germany, September, 2018.
10. F. Grützmacher, A. Hein, P. Lepidis, R. Dorsch, T. Kirste, and C. Haubelt. *Energy Efficient On-Sensor Processing for Online Activity Recognition*. In Proceeding of 3rd International Conference on Pervasive and Embedded Computing (PEC), pp. 85 – 92, Porto, Portugal, July, 2018.
11. M. Rethfeldt, B. Beichler, H. Raddatz, F. Uster, P. Danielis, C. Haubelt, and D. Timmermann. *Mini-Mesh: Practical Assessment of a Miniaturized IEEE 802.11n/s Mesh Testbed*. In Proceedings of the IEEE Wireless Communications and Networking Conference (WCNC), pp. 1 – 6, Barcelona, Spain, April 2018.
12. J.-P. Wolff, S. Stieber, F. Hölzke, D. Gis, C. Haubelt, P. Lepidis, and J. Meier. *Improving Pedestrian Dead Reckoning using Likely and Unlikely Paths*. In Proceedings of Ubiquitous Positioning, Indoor Navigation and Location-Based Services (UPINLBS'18), pp. 59 – 64, Wuhan, China, March 2018. (Best Oral Presentation Award)
13. K. Neubauer, P. Wanko, T. Schaub, and C. Haubelt. *Exact Multi-Objective Design Space Exploration using ASPmT*. In Proceedings of Design, Automation and Test in Europe (DATE), pp. 257 – 260, Dresden, Germany, March, 2018.
14. K. Neubauer, C. Haubelt, P. Wanko and T. Schaub. *Systematic Test Case Instance Generation for the Assessment of System-level Design Space Exploration Approaches*. In

Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV18), Tübingen, Germany, pp. 1-10, March 2018.
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110. G. Bunin, A. Schneider, C. Haubelt, J. Langer and U. Heinkel. *Automatic Test Case Generation with NuSMV*. In Proceedings of the Informatik 2006 - Workshop Modellbasiertes Testen. Dresden, Germany, pp. 262 - 263, October 02-10, 2006.
111. B. Niemann and C. Haubelt. *Formalizing TLM with Communicating State Machines*. In Proceedings Forum on Specification and Design Languages (FDL'06), pp. 285-292, Darmstadt, September 19-22, 2006.
112. J. Falk, C. Haubelt and J. Teich. *Efficient Representation and Simulation of Model-Based Designs in SystemC*. In Proceedings FDL'06, Forum on Design Languages 2006, Darmstadt, Germany, September 19-22, pp. 129 - 134, 2006.
113. T. Streichert, C. Strengert, C. Haubelt and J. Teich. *Dynamic Task Binding for Hardware/Software Reconfigurable Networks*. In Proceedings of SBCCI 2006, pages 38-43, Ouro Preto, Brasil, August 28th - September 1st, 2006.
114. T. Streichert, C. Haubelt and J. Teich. *Multi-Objective Topology Optimization for Networked Embedded Systems*. In Proceedings of the International Conference on Embedded

Computer Systems: Architectures, Modeling, and Simulation (IC-SAMOS 2006), pp. 93--98, Samos (Greece), July 17-20, 2006.
115. J. Keinert, C. Haubelt and J. Teich. *Modeling and Analysis of Windowed Synchronous Algorithms*. In Proceedings of the 31st International Conference on Acoustics, Speech, and Signal Processing (ICASSP2006), Toulouse (France) May 14-19, 2006.
116. D. Koch, T. Streichert, S. Dittrich, C. Strengert, C. Haubelt and J. Teich. *An Operating System Infrastructure for Fault-Tolerant Reconfigurable Networks*. In Proceedings of the 19th International Conference on Architecture of Computing Systems (ARCS 2006), Frankfurt/Main, Germany, pp. 202-216, March 13-16, 2006.
117. M. Streubühr, J. Falk, C. Haubelt, J. Teich, R. Dorsch and T. Schlipf. *Task-Accurate Performance Modeling in SystemC for Real-Time Multi-Processor Architectures*. In Proceedings of Design, Automation and Test in Europe (DATE 2006), IEEE Computer Society, Munich, Germany, pp. 480-481, March 6-10, 2006.
118. T. Schlichter, M. Lukasiewycz, C. Haubelt and J. Teich. *Improving System Level Design Space Exploration by Incorporating SAT-Solvers into Multi-Objective Evolutionary Algorithms*. In Proceedings of IEEE Computer Society Annual Symposium on VLSI. Karlsruhe, Germany, pp. 309-314, March 2-3, 2006.
119. B. Niemann and C. Haubelt. *Assertion-Based Verification of Transaction Level Models*. In Proceedings of the 9th ITG/GMM/GI Workshop, Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, Dresden, Germany, pp. 232-236, February 20-22, 2006.
120. C. Haubelt, M. Jersak, K. Richter, K. Strehl, D. Ziegenbein, R. Ernst, J. Teich and L. Thiele. *SPI-Workbench - Modellierung, Analyse und Optimierung eingebetteter Systeme*. In Proceedings of INFORMATIK 2005 - Informatik LIVE. by Armin B. Cremers, Rainer Manthey, Peter Martini, and Volker Steinhage (Eds.). In Lecture Notes in Informatics. VOL. P-68, No. 2, Bonn, Germany, pp. 693-697, September 19-22, 2005. © Gesellschaft für Informatik, Bonn, Germany, 2005.
121. S. Helwig, C. Haubelt and J. Teich. *Modeling and Analysis of Indirect Communication in Particle Swarm Optimization*. In Proceedings of the 2005 IEEE Congress on Evolutionary Computation, volume 2, pages 1246-1253, Edinburgh, UK, September 2nd-5th, 2005.
122. T. Schlichter, C. Haubelt, F. Hannig and J. Teich. *Using Symbolic Feasibility Tests during Design Space Exploration of Heterogeneous Multi-Processor Systems*. In Proceedings of Application-specific Systems, Architectures and Processors (ASAP). Samos, Greece, pp. 9-14, July 23-25, 2005.
123. T. Schlichter, C. Haubelt and J. Teich. *Improving EA-based Design Space Exploration by Utilizing Symbolic Feasibility Tests*. In Proceedings of Genetic and Evolutionary Computation Conference (GECCO). Washington, DC, pp. 1945-1952, June 25-29, 2005.
124. J. Falk, C. Haubelt and J. Teich. *Representing Models of Computation in SystemC*. In Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen. GI/ITG/GMM-Workshop 2005, Munich, Germany, April 06-07, 2005.
125. T. Dinkel, C. Haubelt, U. Heinkel, T. Schlichter and J. Teich. *Automatische Verifikation von ADeVA-Spezifikationen*. In Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen. GI/ITG/GMM-Workshop 2005, Munich, Germany, April 06-07, 2005.
126. C. Haubelt, J. Gamenik and J. Teich. *Initial Population Construction for Convergence Improvement of MOEAs*. In Evolutionary Multi-Criterion Optimization, Carlos A. Coello Coello, Arturo Hernández Aguirre, and Eckart Zitzler (eds.), Lecture Notes in Computer Science, Vol. 3410, pp. 191-205, Springer, Berlin, Heidelberg, New York, 2005.
127. C. Haubelt. *Automated Model-Based Design Space Exploration of Embedded Systems*. PhD Forum at the Design, Automation and Test in Europe (DATE'05), March 7-11, Munich, Germany, 2005.
128. T. Streichert, C. Haubelt and J. Teich. *Distributed HW/SW-Partitioning for Embedded Reconfigurable Systems*. In Proceedings of DATE 2005, Munich, Germany, pp. 894-895, March 7-11, 2005.
129. T. Streichert, C. Haubelt and J. Teich. *Verteilte HW/SW-Partitionierung für fehlertolerante rekonfigurierbare Netzwerke*. In Proceedings of 17. ITG/GI/GMM Workshop für Testmethoden und Zuverlässigkeit und Fehlertoleranz von Schaltungen und Systemen. Innsbruck, Austria, pp. 50-54, February 27 - March 1, 2005.
130. C. Haubelt, S. Otto, C. Grabbe and J. Teich. *A System-Level Approach to Hardware Reconfigurable Systems*. In Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC'05). Shanghai, China, pp. 298-301, January 18-21, 2005.

131. T. Streichert, C. Haubelt and J. Teich. *Online Hardware/Software Partitioning in Networked Embedded Systems*. In Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC'05). Shanghai, China, pp. 982-985, January 18-21, 2005.
132. C. Haubelt. *Design Space Exploration for Distributed Hardware Reconfigurable Systems*. In Field-Programmable Logic and Applications by Jürgen Becker, Marco Platzner, and Serge Vernalde (Eds.). In Lecture Notes in Computer Science, Vol. 3203, p. 1171, Springer, Berlin, Heidelberg, 2004.
133. C. Haubelt, D. Koch and J. Teich. *Basic OS Support for Distributed Reconfigurable Hardware*. In Proceedings of the International Workshop on Systems, Architectures, Modeling and Simulation (SAMOS'04), Samos, Greece, July 19-21, published as Springer Lecture Notes in Computer Science (LNCS), volume 3133, pages 30-38, 2004.
134. C. Haubelt and J. Teich. *Accelerating Design Space Exploration*. In Proceedings of 5th International Conference on ASIC (ASICON 2003), pp. 79-84, Beijing, China, October 21-24, 2003.
135. C. Haubelt, D. Koch and J. Teich. *ReCoNets: Modeling and Implementation of Fault Tolerant Distributed Reconfigurable Hardware*. In Proceedings of the 16th Symposium on Integrated Circuits and Systems Design (SBCCI2003), pp. 343-348, São Paulo, Brazil, September 8-11, 2003.
136. R. Feldmann, C. Haubelt, B. Monien and J. Teich. *Fault Tolerance Analysis of Distributed Reconfigurable Systems Using SAT-Based Techniques*. In Proceedings of 13th International Conference on Field Programmable Logic and Applications, pp. 478-487, Lisbon, Portugal, September 1-3, 2003.
137. C. Haubelt, D. Koch and J. Teich. *Basic OS Support for Distributed Reconfigurable Hardware*. In Proceedings of the Third International Workshop on Systems, Architectures, Modeling and Simulation (SAMOS'03), pp. 18-22, Samos, Greece, July 21-23, 2003, ISBN 90-807957-1-2.
138. C. Haubelt, S. Mostaghim, J. Teich and A. Tyagi. *Solving Hierarchical Optimization Problems Using MOEAs*. In Evolutionary Multi-Criterion Optimization, Carlos M. Fonseca, Peter J. Fleming, Eckart Zitzler, Kalyanmoy Deb, and Lothar Thiele (eds.), Lecture Notes in Computer Science, Vol. 2632, pp. 162-176, Springer, Berlin, Heidelberg, New York, 2003.
139. C. Haubelt, J. Teich, R. Feldmann and B. Monien. *SAT-Based Techniques in System Synthesis*. In Proceedings of Design, Automation and Test in Europe (DATE 2003), Norbert Wehn and Diederik Verkest, IEEE Computer Society, Munich, Germany, pp. 1168-1169, March 3-7, 2003.
140. C. Haubelt and J. Teich. *Accelerating Design Space Exploration Using Pareto-Front Arithmetics*. In Proceedings ASP-DAC 2003, Asia and South Pacific Design Automation Conference, pp. 525-531, Kitakyushu, Japan, January 21-24, 2003.
141. C. Haubelt, J. Teich, K. Richter and R. Ernst. *System Design for Flexibility*. In Proc. DATE 2002, Design, Automation and Test in Europe, IEEE Computer Society Press, pp. 854-861, Paris, France, March 4-8, 2002.
142. C. Haubelt, J. Teich, K. Richter and R. Ernst. *Modellierung Rekonfigurierbarer Systemarchitekturen*. GI / ITG / GMM Workshop - Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, Tuebingen, Germany, Shaker Verlag, pp. 163-171, February 25-27, 2002.

Non-Reviewed Journal Articles:

1. A. Hein, F. Grützmacher, C. Haubelt, T. Kirste, *Fast Care – Real-Time Sensor Data Analysis Framework for Intelligent Assistance Systems*. In Journal on Current Directions in Biomedical Engineering, Vol. 3, Nr. 2, pp. 743–747, September 2017.
2. C. Haubelt, J. Teich and R. Dorsch. *Entdecke die Möglichkeiten*. In Design&Elektronik (8):22-27, 2008, WEKA.

Non-Reviewed Conference Papers:

1. J.-P. Wolff, F. Grützmacher, R. Dorsch, R. Kaack, L. Middendorf, and C. Haubelt. *Towards Automated Prototyping of Gesture Recognition Systems for Wearable Devices using Inertial Sensors*. In Proceedings of Smart Systems Integration, Barcelona, Spain, pp. 85-92, April, 2019. (Best Paper Award Nominee)
2. N. Büscher, M. Stieringer, and C. Haubelt*, Evaluation Method for the absolute Orientation from the Rotation Vector on Mobile Devices.* In Proceedings of the IEEE International

Symposium on Inertial Sensors and Systems (INERTIAL), Naples, Florida, USA, pp. 179-183, April, 2019.

3. M. Geilen, J. Falk, C. Haubelt, T. Basten, B. Theelen, S. Stuijk. *Performance Analysis of Weakly-Consistent Scenario-Aware Dataflow Graphs*. In Proceeding of the Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, CA, U.S.A.,pp. 393-397, 2014.
4. C. Haubelt, F. Ludwig, L. Middendorf, and C. Zebelein. *Using Stream Rewriting for Mapping and Scheduling Data Flow Graphs onto Many-Core Architectures*. In Proceeding of the Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, CA, U.S.A., pp. 1431-1435, 2013.
5. P. Kutzer, M. Streubühr, C. Haubelt, J. Teich and A. von Schwerin. *Actor-oriented Modeling of Industrial Ethernet in the Automation Domain Using SystemC*. Proceedings of the Embedded World Conference, Nuremberg, Germany, 2011.
6. M. Streubühr, M. Jäntsch, C. Haubelt and J. Teich. *From Model-based Design to Virtual Prototypes for Automotive Applications*. In Proceedings of the Embedded World Conference, Nuremberg, Germany, March 03-05, 2009.
7. A. Schneider, G. Bunin, C. Haubelt and U. Heinkel. *Automatic Test Generation with Model Checking Techniques*. In Software Quality in Service-Oriented Architectures Proceedings of the Conference on Quality Engineering in Software Technology (CONQUEST2006). Berlin, Germany, pp. 307 - 318, September 27-29, 2006.
8. T. Dinkel, C. Haubelt, U. Heinkel, J. Knäblein, T. Schlichter, S. Schock and J. Teich. *Comparison of Techniques for the Automatic Verification of ADeVA Specifications*. In Dresdener Arbeitstagung Schaltungs- und Systementwurf (DASS 2005). Dresden, Germany, April 13-14, 2005.
9. C. Haubelt and J. Teich. *Modeling and Analysis of Distributed Reconfigurable Hardware*. In Dresdener Arbeitstagung Schaltungs- und Systementwurf (DASS 2004), pp. 106-111, Dresden, Germany, April 19-20, 2004.
10. M. Jersak, K. Richter, D. Ziegenbein, R. Ernst, C. Haubelt, F. Slomka and J. Teich. *SPI-Workbench für die Analyse eingebetteter Systeme*. Workshop: Modelle, Werkzeuge und Infrastrukturen zur Unterstützung von Entwicklungsprozessen, Aachen, Germany, March 20-22, 2002.

Invited Talks:

1. K. Neubauer, P. Wanko, T. Schaub, and C. Haubelt. *Application Mapping and Scheduling through ASPmT with Partial Assignment Evaluation*, at the 20th International Workshop on Software and Compilers for Embedded Systems (SCOPES'17), June 15, Sankt Goar, Germany, 2017.
2. C. Haubelt, *Designing Embedded MEMS-Based Activity Recognition Systems*, at the 3rd international Workshop on Sensor-based Activity Recognition and Interaction (iWOAR'16), June 24, Rostock, Germany, 2016.
3. F. Grützmacher, B. Beichler, B. Theelen, and C. Haubelt. *Performance Estimation of Template-based Gesture Recognition on Multi- Core Architectures Using Scenario-Aware Dataflow Graphs*. At Integrating Dataflow, Embedded computing and Architecture (IDEA'2016) Workshop. April 11, Vienna, Austria, 2016.
4. C. Haubelt: *Gesture Detection On-Loading for the Next Generation Sensor Subsystems*. At TISU: Transfer to Industry and Start-Ups, January 19, Prague, Czech Republic, 2016.
5. C. Haubelt. *A Novel Task Mapping Approach Based on Stream Rewriting*. Invited Talk at KTH Stockholm, December 5, Stockholm, Sweden, 2014.
6. A. Nitsch, B. Beichler, F. Golatowski, and C. Haubelt. *Towards a Model-based Design for ETCS Speed and Distance Monitoring*. At Internationale Fachmesse für Verkehrstechnik - Innovative Komponenten, Fahrzeuge, Systeme (InnoTrans 2014), September 24, Berlin, Germany, 2014.
7. C. Haubelt. *A Novel Task Mapping Approach Based on Stream Rewriting*. Invited Talk at Eindhoven Technical University, October 24, Eindhoven, The Netherlands, 2013.
8. R. Kiesel, O. Löhlein, M. Streubühr, J. Teich, and C. Haubelt. *SystemC-based Actor-oriented Modeling of an Automotive Pedestrian Detection System*. At 24. European SystemC User's Group Meeting, September 13, Oldenburg, Germany 2011.
9. C. Haubelt. *Synthesis and Optimization of Heterogeneous Multi-Core Systems*. Invited Talk at Eindhoven Technical University, December 9, Eindhoven, The Netherlands, 2010.

10. C. Haubelt. Accelerated *Design Space Exploration for Heterogeneous MPSoCs Using Symbolic Techniques.* At ARTIST Design Map2MPSoC 2010 Workshop, June 29, St. Goar, Germany, 2010.
11. C. Haubelt. *ESL Synthesis Across Hardware/Software Boundaries*. Invited Talk at the Workshop on Compiler-Assisted System-On-Chip Assembly (CASA'09), Embedded Systems Week 2009, October 10, Grenoble, France, 2009.
12. C. Haubelt. *SystemCoDesigner: An ESL Synthesis Methodology*. DATE´09 Friday Workshop: The Future of ESL Synthesis, Nice, France, 2009. Invited Talk.
13. M. Streubühr, C. Haubelt and J. Teich. *System Level Performance Simulation for Heterogenous Multi-Processor Architectures*. 1st Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO), in conjunction with the 4th HiPEAC Conference, Paphos, Cyprus, January 25, 2009.
14. C. Haubelt. *An Actor-Oriented Design Methodology Using SystemC*. Invited talk at IBM Future Technology Forum, Böblingen, Germany, December 12, 2008.
15. C. Haubelt. *SystemCoDesigner - Map2MPSoC 2008*. Invited talk at ARTIST Design Map2MPSoC 2008 Workshop, Düsseldorf, Germany, November 28, 2008.
16. C. Haubelt. *SystemCoDesigner - A Methodology for an Early Assessment of Design Options*. Invited talk at the Fraunhofer Institut für Integrierte Schaltungen (FhG-IIS), Erlangen, Germany, November 25, 2008.
17. C. Haubelt, J. Falk, C. Zebelein, J. Keinert, J. Teich and S. Bhattacharyya. S*ystemCoDesigner - An ESL Design Methodology Based on the FunState MoC*. Talk at 2nd Artist Workshop on Models of Computation and Communication, Eindhoven, The Netherlands, July 3, 2008.
18. C. Haubelt. *SystemCoDesigner: Automatic Design Space Exploration and Rapid Prototyping from Behavioral Models*. Talk at Center of Embedded Computer Systems, Irvine, CA, USA, June 13, 2008.
19. C. Haubelt. *SystemCoDesigner - A Methodology for an Early Assessment of Design Options*. Invited Talk at the 1. ILP-Summit Embedded Systems Institute, Nuremberg, Germany, February 27, 2008.
20. C. Haubelt. *Substantiating Early Design Decisions by Automatic Design Space Exploration*. Invited Talk at TU Chemnitz. December 12, Chemnitz, Germany, 2007.
21. J. Falk, J. Gladigau, C. Haubelt, J. Keinert, T. Schlichter, M. Streubühr and J. Teich. *Substantiating Early Design Decisions by Automatic Design Space Exploration*. Talk at 16. European SystemC Users Group Meeting, September 18, Barcelona, Spain, 2007.
22. J. Falk, J. Gladigau, C. Haubelt and J. Teich. *SysteMoC - Verification and Refinement of Actor-Based Models of Computation*. Talk, ARTIST2 Workshop on MoCC - Models of Computation and Communication, November 16-17, Zurich, Switzerland, 2006.
23. C. Haubelt. *SystemCoDesigner - Eine Entwurfsmethodik für SystemC-Beschreibungen*. Invited Talk, Siemens Medical Solutions, July 17, Erlangen, Germany, 2006.
24. C. Haubelt. *SystemCoDesigner - Eine Entwurfsmethodik für SystemC-Beschreibungen*. Invited talk, Institute of Computer and Communication Network Engineering, TU Braunschweig, April 28, Braunschweig, Germany, 2006.
25. C. Haubelt. *SystemCoDesigner - Eine Entwurfsmethodik für SystemC-Beschreibungen*. Invited Talk, Oldenburger Forschungs- und Entwicklungsinstitut für Informatik-Werkzeuge und Systeme OFFIS, April 24, Oldenburg, Germany, 2006.
26. J. Teich, C. Haubelt, D. Koch and T. Streichert. *Concepts for Self-Adaptive Automotive Control Architectures*. DATE'06 Friday Workshop Future Trends in Automotive Electronics and Tool Integration, Conference Design Automation and Test in Europe, March 10, 2006, Munich, Germany.
27. C. Haubelt. *Eine modellbasierte Entwurfsmethodik für SystemC*. Invited talk, Professur Schaltkreis- und Systementwurf, TU Chemnitz, February 1, Chemnitz, Germany, 2006.
28. C. Haubelt. *SystemCoDesigner: Entwurfsraumexploration für SystemC-Beschreibungen*. Invited Talk, Fraunhofer Institut für Integrierte Schaltungen (FhG-IIS), December 12, Erlangen, Germany, 2005.
29. C. Haubelt. *A System-Level Approach to Automated Model-Based Design Space Exploration*. Invited Talk at the Computer Engineering and Networks Laboratory (TIK), ETH Zurich, March 31, Zurich, Switzerland, 2005.
30. C. Haubelt. *Introduction to Hardware-Software-Co-Design*. Invited Talk, Fraunhofer Institut für Integrierte Schaltungen (FhG-IIS), May 03, Erlangen, Germany, 2004.
31. C. Haubelt. *Hierarchische Mehrzieloptimierung Eingebetteter Systeme*. Invited Talk, Oldenburger Forschungs- und Entwicklungsinstitut für Informatik-Werkzeuge und Systeme OFFIS, September 16, Oldenburg, Germany, 2003.

Tutorials:

1. C. Haubelt. *Entwurf und virtuelles Prototyping*. Kompaktkurs "Eingebettete Systeme", May 7th, Rostock, Germany, 2014.
2. C. Haubelt. *Integrated Finite State Machine and Dataflow Modeling*. Lecture at the Summer School on Models for Embedded Signal Processing Systems, September 2nd, Leiden, The Netherlands, 2010.
3. C. Haubelt. *Designing Heterogeneous MPSoCs*. DAC'10 Friday Tutorial "SystemC for Holistic System Design with Digital Hardware, Analog Hardware, and Software". June 18th, Anaheim, CA, U.S.A., 2010.
4. C. Haubelt. *Designing Multi-Processor Systems-on-Chip*. Embedded Tutorial at the 22nd International SoC Conference. September 10th, Belfast, Northern Ireland, UK, 2009.
5. J. Teich and C. Haubelt. *Principles: Analysis, Optimization and Exploration*. DATE´09 Monday Tutorial: System-Level Modeling, Analysis and Synthesis of Embedded Multi-Core Designs, Nice, France, 2009. Invited Talk.
6. C. Haubelt. *Practice: ESL Case Studies (Motion-JPEG Example)*. DATE´09 Monday Tutorial: System-Level Modeling, Analysis and Synthesis of Embedded Multi-Core Designs, Nice, France, 2009. Invited Talk.
7. C. Haubelt and B. Niemann. *Formalizing and Verifying SystemC TLMs*. Talk at FDL Industrial Workshop on Verification of Complex Systems, September 19, Barcelona, Spain, 2007.
8. C. Haubelt. *Hardware-Software-Partitioning with SystemC*. In Master Course Modern Design Techniques with SystemC at the Design, Automation and Test in Europe (DATE'04), February 20, Paris, France, 2004.