Redesign of the FSM module of the Trigger-Time-Event (TTE) System

- Language: German or English

- Prerequirements:
  - VHDL/Verilog programming and testing
  - Benefical: Experience with Xilinx ISE

- Tasks:
  - Familiarise with the Wendelstein 7-X TTE project
  - Redesign of the FSM module (Moore machine):
    - Can implement an arbitrary FSM in HW
    - Configurable via Ethernet interface
    - Increase of the configuration intuitiveness (e.g. by dynamic transition planning)
  - Creation of a test bench and comprehensive proof of functionality
  - Documentation of all steps

- Literature:
  - Max Planck Institute for Plasma Physics: https://www.ipp.mpg.de/
  - TTE: https://ieeexplore.ieee.org/document/7543115
  - More material will be provided

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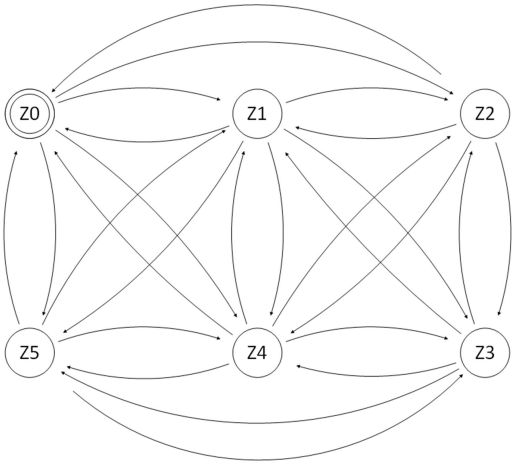

Example of dynamic transition planning

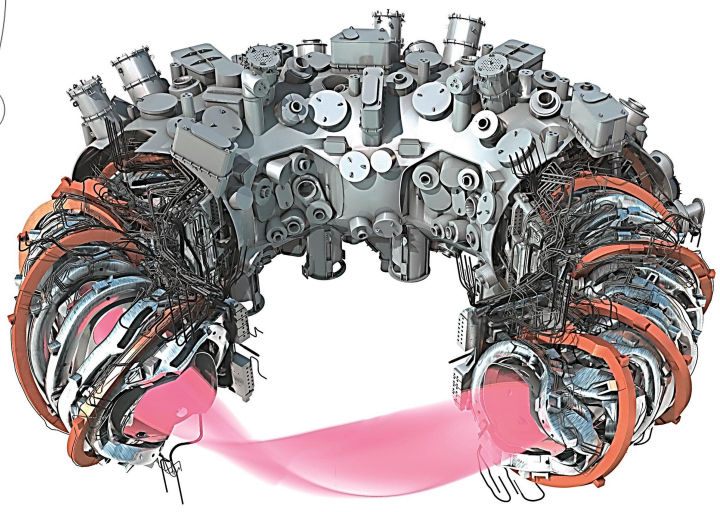

Illustration: ipp.mpg.de