Universität Rostock

Traditio et Innovatio

**Topic for a Bachelor/Master/Pre-Thesis, Master Project,
or to work on as a Student Research Assistant**

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Design of a testbed for investigation of clock stability and time synchronicity of networked devices

The need for a common time base among elements and devices in networks is becoming increasingly important. Furthermore, time-critical applications in telecommunications, smart power grids, data centers, industrial automation, and time-sensitive and distributed computing networks are demanding decreasing time variations between networked devices.

Besides accuracy and reliability, the main requirements for time synchronization solutions are robustness against hardware or network errors and failures as well as any kind of system attacks. Besides the high effort to verify the fulfillment of these requirements, it is almost impossible to represent a real system in its entirety as a software model in order to obtain exact simulation results.

In order to test and improve existing approaches to time synchronization and to explore the influence of environmental conditions on the system clock, a test environment with physical devices must be developed. Suitable platforms for these requirements are for example the Zedboard with the Xilinx Zynq-7000 SoC or the ZCU102 Evaluation Kit with the Xilinx Zynq UltraScale+ MPSoC, which has both a general purpose CPU and an FPGA part. A system developed by the company Xillybus (http://www.xillybus.com/) especially for Xilinx Zynq and Intel Cyclone V architectures allows direct communication of a customized, Ubuntu-Based Linux with the FPGA part of the SoC.

Summarized, the following tasks have to be solved:

- Read into the basics of time synchronization
  (e.g., https://www.ni.com/de-de/innovations/white-papers/12/synchronization-basics.html)

- Get the Xillybus demo bundle from the website and get both boards running with it
  (http://xillybus.com/xillybus-lite)

- Install Linux-PTP (http://linuxptp.sourceforge.net/), connect both evaluation boards via Ethernet
  (switch required when controlling the boards via ssh) and establish initial time synchronisation between them

- Become familiar with existing testbed approaches (e.g., https://ieeexplore.ieee.org/document/9334990)
  and derive an own concept to measure and compare clock stability on the FPGA side

- Implement a prototype and validate it experimentally

- Create a git repository, upload all project files and write a short project description

- Create a detailed documentation of all work steps

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