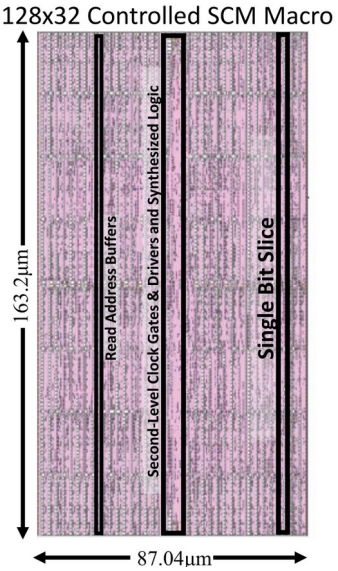
Universität Rostock
Traditio et Innovatio
Fakultät für Informatik und Elektrotechnik
Institut für Angewandte Mikroelektronik und Datentechnik

Project-/Specialization Module, Master Thesis

Controlled Synthesis of Standard Cell Memory Arrays

Within the Collaborative Research Centre 1270 ELAINE (ELectrically Active ImplaNts) the team at IMD does research on an energy-efficient implant platform to enable feeback-controlled electrical stimulation.
Currently investigated microcontroller architectures for an implant ASIC make use of wide-range voltage scaling, featuring supply voltages in the sub- and near-threshold voltage region of transistors, to reduce the dynamic power dissipation. Generic static random access memories (SRAMs) - which are supplied by third-party vendors - do not scale the same way as logic gates and limit the lower voltage range.
As an alternative, standard cell memories (SCMs) can be defined, synthesized, placed and routed as part of the rest of the digital design, providing complete design flexibility, better energy-efficiency at small sizes and low-voltage operation.

Recent publications present optimized physical implementations of SCMs using a controlled placement methodology in the standard design flow with commercial electronic design automation (EDA) tools. Since this methodology partly depends on the underlying CMOS technology, it must be adapted to our target silicon process.



Thus, the following tasks have to be conducted:

- Literature research and familiarization with the design methodologies and EDA tools
- Implementation of a Latch-based memory array in a Hardware Description Language (Verilog or VHDL) using an existing design description
- Define constraints and directives scripts for the synthesis and physical implementation steps
- Evaluation and discussion of results
- Documentation of the work

The scope of the tasks depends on the applied module (PA/SM/MT) and group size.

Prerequisite:

- Successfully completed the course Advanced VLSI Design
- Basic understanding of the EDA flow and digital designs
- Basic understanding of VHDL/Verilog, TCL or any other shell scripting language

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