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Universität Rostock
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Specialization Module/Master project

Functional Property Checking with Answer Set Programming

[Problem Description]

Embedded systems are nowadays ubiquitous in daily life. They are integrated in larger systems and employed in many different sectors. Accordingly, the constraints that are put upon the embedded systems are also various. In order to guarantee that an embedded system is designed as intended, its functional properties has to be verified. This is done by *functional property checking,* a process that utilizes temporal logics to encode functional constraints of state-full systems. For example, a systems that must always be able to always reach its initial state (s_0) has to conform to the constraint AGEF(s_0).

There are essentially two major temporal logics: *computation tree logic* (CTL) and *linear time logic* (LTL). They differentiate mostly in their interpretation of time. While CTL has a branching time leading to potentially different successors per state, LTL assumes a linear time where every state has exactly one successor.

Answer Set Programming (ASP), on the other hand, is a knowledge representation framework based on the *stable model semantics*. It used to encode a problem into a logic program whose stable models than represent the solution of the initial problem. This has proven to be effective in various areas – especially for mapping and allocation problems emerging during the design of embedded systems.

In this work, it shall be investigated whether ASP can be utilized for the verification of functional properties of a system. Therefore, an extensive literature research has to be done. Approaches are then to be implemented and tested on varying examples.

[Prerequisites]

- Selected Topics in Embedded Systems Design or similar module
- Basic understanding in SAT/ASP/ILP

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