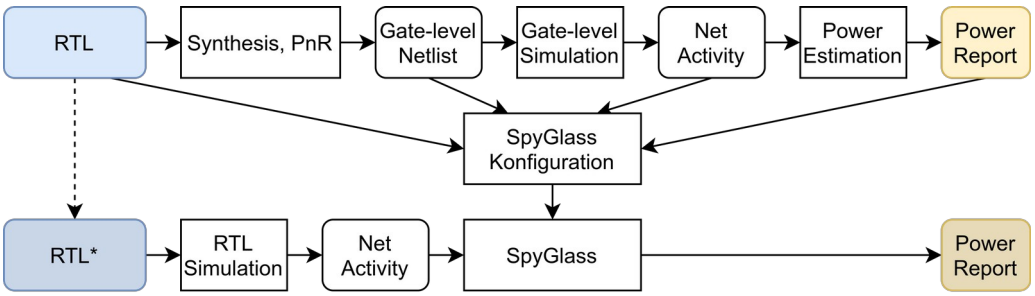
Universität Rostock
Traditio et Innovatio
Fakultät für Informatik und Elektrotechnik
Institut für Angewandte Mikroelektronik und Datentechnik

Project/Specialization Module

VLSI Power Estimation and Exploration on Register Transfer Level

Power dissipation and energy efficiency have become a major constraint in many application-specific integrated circuit (ASIC) designs. Accurate estimations that are close to real measurements on silicon are possible near the end of the design cycle with a physically implemented design and expensive simulations.
Design decisions on a system and micro-architectural level have a great impact on the resulting power dissipation of the physical implementation, while the optimization techniques during later design stages are very often limited by other constraints. Therefore, it is of interest to have an accurate power estimation during early design stages to explore different power architectures and to evaluate alternative micro architectures.

The program *SpyGlass* of the electronic design automation company *Synopsys* advertises to include accurate, timing and synthesis aware power estimation for design descriptions on register transfer level (RTL). Moreover, the accuracy can be enhanced by a calibration procedure which uses an already physically implemented design.



During the time of the project or specialization module following tasks have to be conducted:

- Familiarization with power estimation methodologies and *Synopsys Spyglass*
- Establish a workflow for RTL power estimation with Spyglass
- Evaluate estimation accuracy using various designs
- Evaluate estimation accuracy improvements through design and tool calibration
- Documentation of the work

Prerequisite:

- Basic understanding and experience with any HDL (Verilog or VHDL)
- Basic knowledge of TCL or similar scripting languages

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