Student Assistent Job

Establishment of a Modular ASIC Tool Flow Automation

Today, the design of application-specific integrated circuits (ASICs) relies on well established design methodologies using electronic design automation (EDA) tools. The design flow includes various steps like design conceptualization, chip architecture optimization, logical/physical implementation and design validation. Although the process must be adapted to the designs needs within each project, the fundamental flow remains unchanged. Both commercial and open-source EDA programs are highly sophisticated tools, which can be controlled by scripting interfaces and allow extensive automation.

To improve the quality of results and speed up future research and development of integrated circuits, a base ASIC flow automation is to be established. For this an existing open-source modular flow specification and build-system generator for ASIC and FPGA design-space exploration is used and must be extended. During the position as student assistant you will help to improve and integrate missing crucial steps of the flow and gain experience and know-how working with industry standard EDA software from Synopsys, Cadence and Mentor.

Currently following exemplary tasks have to be addressed:

- Adapting the physical implementation steps using Cadence Innovus to the target 65 nm CMOS process
- Integration of an automated RTL and netlist simulation step using Mentor Modelsim
- Integration of a static power analysis step using Synopsys tools
- Adapting the automated ASIC flow to be used within a current SoC design project

Prerequisite:
- Basic understanding of the ASIC design flow
- Some experience with EDA tools, preferably completed the course *Advanced VLSI Design*
- Basic knowledge of TCL or similar scripting languages
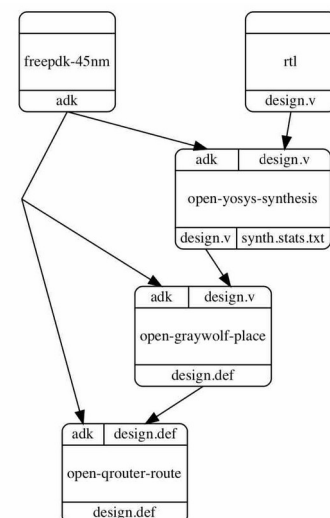
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