Selected Topics in VLSI Design

Project Presentation

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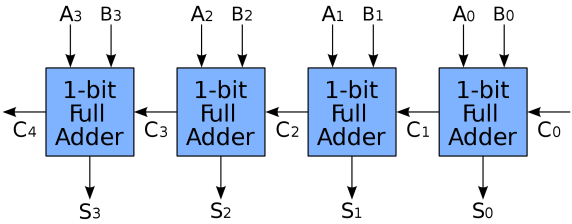
Adder Structure

- n-bit input (two's complement)
- carry propagate adder
- n-bit ripple carry adder

$$Area = 7 * n$$

$$Time = 2 * n$$



Multiplier

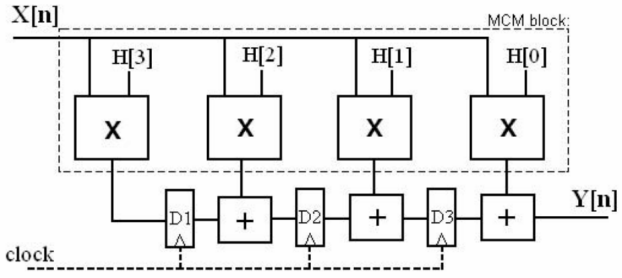
- n*m bit input (two's complement)
- Signed Pezaris Array Multiplier

$$Area = O(n^2)$$

$$Time = O(n)$$

	$1001 * 1101$ ($decimal: -7 * -3$)	
+	11111001	($1001 * 1$, *sign extension*)
+	0000000	($1001 * 0$, *sign extension*, left-shift)
+	111001	($1001 * 1$, *sign extension*, left-shift)
−	11001	($1001 * 1$, *sign extension*, left-shift)
	00010101 ($decimal: +21$)	

Optimization-Structure



Daitx F.,Rosa V.,Costa E.,Flores P.,Bampi S. 2008 VHDL Generation of Optimized FIR Filters , 2008 International Conference on Signals, Circuits and Systems.

Optimization

- Number representation
- faster and smaller CPA adder
- Pipelining
- booth- booth/wallace multiplier