Improving Calibration Precision of Signal-Delay-Based Time Measurement Systems in FPGAs

Ralf Joost, Matthias Hinkfoth, and Ralf Salomon
Faculty of Computer Science and Electrical Engineering
University of Rostock
18051 Rostock, Germany
email: {ralf.joost},{matthias.hinkfoth}, {ralf.salomon}@uni-rostock.de

***Abstract*— For inherent technical reasons, most asynchronous time measurement systems, such as tapped delay lines and BOUNCE, yield superior resolutions than the synchronous counterparts. However, for high performance systems with a resolution of 10 ps or below, the calibration process is involving, tedious, and error prone. This paper shows that with the integration of another asynchronous phase shift detector, called X-ORCA, the calibration process becomes more reliable and surprisingly easy.**

Keywords—FPGA, Time Interval Measurement, Precision

I. INTRODUCTION (*Heading 1*)

In the field of high-precision time measurement, tapped delay lines (TDL) constitute a de facto standard [1]. Normally, a tapped delay line consists of a chain of sequentially connected flip flops (or latches). In addition, a tapped delay line features two distinct control inputs, called start signal and stop signal. The start signal is connected to the chain's first flip flop and has to travel through all the flip flops one by one. The stop signal, by contrast, is connected to the entire chain such that this signal arrives at all flip flops at the same time. Due to this internal architecture, a tapped delay line essentially counts the number of chain elements through which the start signal has rippled before the stop signal arrives. A rough sketch of a tapped delay line is presented in Fig. 1. For a more in-depth introduction into tapped delay lines, the interested reader is referred to the pertinent literature [2].

From the description presented above, the following key feature of tapped delay lines should become apparent: the internal delay Δt within each flip flop (or alternate active delay element) determines a tapped delay line's resolution.

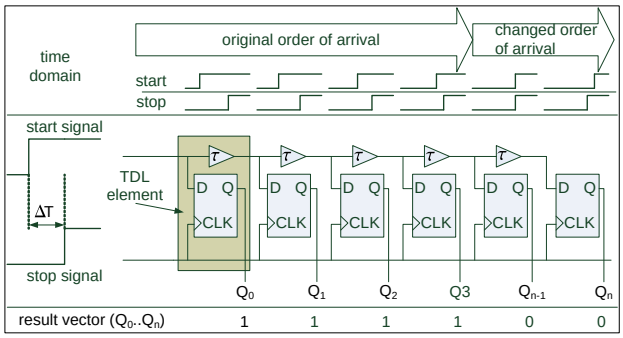

Fig. 1. Basic principle of operation of a Tapped Delay Line (TDL)

The reason is simple: on average, it takes the start signal Δt time to travel from one flip flop to the next one. It should be furthermore evident that this internal delay Δt is technology dependent as it is limited by a semiconductor's fabrication process. With current technologies, state-of-the-art tapped delay lines yield a resolution in the area of 10-50 ps [3].

Recent research [4] has proposed an alternative architecture, which has been named BOUNCE (bunch of unconnected chain elements). In way contrast to tapped delay lines, BOUNCE connects both the start and the stop signal *directly* to the involved flip flops (or latches). However, a key feature is that all the wires have different lengths, which in turn impose different internal delays ε_i to both signals. These internal delays do *not* depend on the semiconductor's technology parameters but purely on the wire lengths on which the signals travel with approximately two third of the speed of light *2/3* c_0. A suitable positioning scheme places all involved flip flops across the device (e.g., an FPGA or ASIC). All flip flops are connected by two anti-parallel wires. An architectural sketch is presented in Fig. 2. A prototypical implementation on a rather vintage StratixII FPGA achieves a resolution of about 10 ps.

Section II presents a brief review of the BOUNCE architecture as far as necessary for the understanding of this paper; for further details, the interested reader is referred to the pertinent literature [5]. Even though every single BOUNCE element provides a decision only about whether or not the start signal has arrived before or after the stop signal, the number of

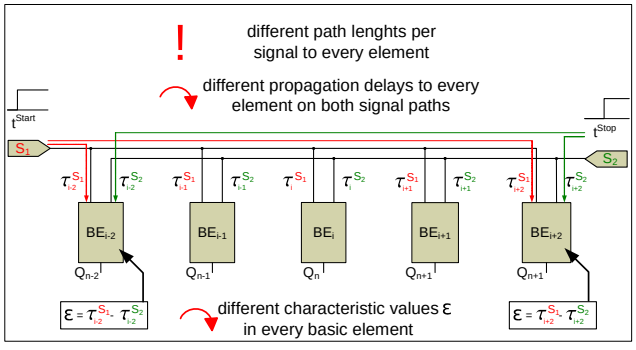

Fig 2. The BOUNCE approach: placing latches at different positions to yield different propagation delays.

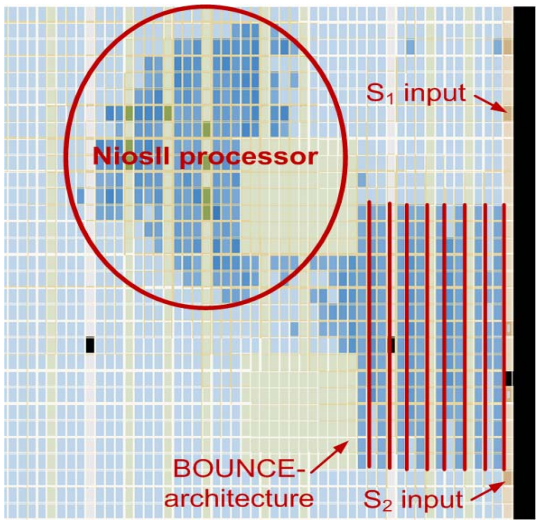

Fig. 3. On-Chip layout of BOUNCE: 1024 detectors are placed in the right side of the chip. Picture taken from Alteras FPGA synthesis tool.

positively set flip flops still represents the duration of the time interval defined by these two signals. Since the resolution of BOUNCE does not depend on any internal, technology-dependent gate delay but on the length of the internal wire lengths, both the actual placement and the chosen wire routing is of particular importance for the accuracy of the time measurement result. Therefore, BOUNCE requires the execution of an initial, one-time calibration procedure. Because BOUNCE's resolution is much better than the precision of the vast majority of the available standard laboratory equipment, the calibration procedure is quite tricky and error prone. Some of these issues are reviewed in Section III.

Recent research [6] has developed a variation of BOUNCE that does not measure the duration of a (one-time) time interval but the phase shift of two identical periodic signals. This system has been named X-ORCA and yields a phase shift resolution of about 10 ps on a CycloneII FPGA for signal frequencies of up to 300 MHz. In comparison to BOUNCE, X-ORCA has the advantage of a very simple, easy-to-perform calibration procedure.

The main idea of this paper is to implement a hybrid of both systems, BOUNCE and X-ORCA in which the former is responsible for the time measurements whereas the latter performs BOUNCE's calibration procedure. The details as far as relevant for the understanding of this paper are all presented in Section IV.

This hybrid has been realized in a prototypical implementation on an Altera CycloneII FPGA. In order to allow for a third-party reproduction of the presented results,

Section V presents all the implementation details as well as a description of the physical/experimental setup. The results, as presented in Section VI, indicate that the proposed calibration approach improves precision of the timing measurement system from 170 ps to 20 ps in comparison to the standard calibration procedure applied so far. Finally, Section VII concludes this paper with a brief discussion.

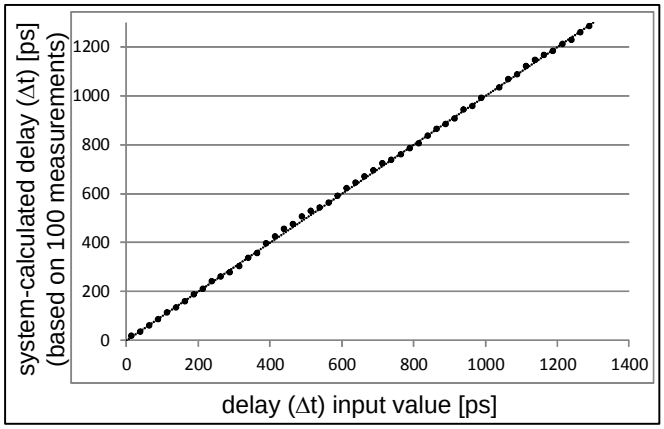

Fig. 4. BOUNCE' results of delay measurements.

II. Background: The BOUNCE Architecture

BOUNCE [4] was developed for measuring the time difference between two events, which can also be interpreted as the duration of a time interval defined by two signals called start S_1 and stop S_2. The two signals S_1 and S_2 can originate from any physical phenomenon, such as the arrival of radio signals at two different receivers, the length of an electrical wave form, or any other trigger.

The general technical approach is that in contrast to synchronous systems, such as high frequency counters, BOUNCE consists of a rather moderate number (e.g., 1000) of independently (asynchronously) operating event detectors that are implemented as standard RS flip flops. Depending on both the (internal) wire lengths and the actual timing of the start and stop signals, every flip flops comes to an individual decision whether or not the start signal appeared before or after the stop signal. In case the internal delays, caused by the internal wire lengths as well as the electrical characteristics of every flip flop, are known, such an asynchronous system constitutes a high-precision time measurement system.

It should be obvious that all the internal time delays should be as diverse as possible; otherwise all flip flops would always be coming up with the same result, which would be totally useless. This design goal can be easily obtained by the following two design constraints: (1) All the flip flops should be spatially distributed across the available digital device, and (2) the start and stop signals should be fed into the circuitry at opposing ends. These two design constraints lead to most varying internal time delays, and thus a high resolution and a decent effective range.

The general on-chip layout of a suitable BOUNCE implementation is shown in Fig. 3. Here, 1024 flip flops were placed in 8 rows of an Altera StratixII FPGA. A NIOSII soft-core processor controls the BOUNCE system and transfers the results to a PC for visualization. This system yields a resolution of approximately 10 ps [5].

Fig. 4 shows the results gained by an experiment were different delays Δt were applied to the system. The calculation

of the results basically involves counting the number of flip flops exhibiting a logical 1 output. As can be seen, the system output follows the desired behavior. In a prior calibration phase, the system stores the number of flip flops that should provide a logical 1 for a set of known delay values. During measurements, the number of logical-1 values found in the output of all flip flops is compared to those values from calibration. Due to this comparison, the calibration process has to be as precise as possible. However, the precision of the calibration is limited by the problems that are in focus of the following section.

III. Problem Description

It has already been discussed above that BOUNCE consists of a moderate number of individually (asynchronously) operating flip flops that are distributed across an implementation device. It has furthermore been outlined that every single flip flop merely determines, which of the two signals arrives earlier than the other one. Finally, it has been discussed that the decision of every single flip flop not only depends on the initial timing of the start and stop signal but also on the internal delays which are mainly technology and thus implementation dependent. Hence, asynchronous systems, such as BOUNCE, require a solid calibration process in order to exploit their inherent performance capabilities.

Since the time resolution of BOUNCE is way better than regular laboratory equipment, all the implemented flip flops have to be calibrated by hand, one by one. Due to natural reasons, this process is tedious, cumbersome, and error prone. The straight-forward approach [4] is as follows:

1. One of the available output ports of a signal generator is connected to a splitter, which in turn is connected via two separate wires with both the start and the stop inputs S_1 and S_2.
2. One of the wires has constant length, whereas the other one incorporates a line stretcher [7] that can be adjusted at varying lengths.
3. By *slightly* changing the length of the line stretcher, the calibration process has to determine the external delay for which a chosen flip flops yields both logical values with equal probability.

This process is notoriously time consuming. Due to technical reasons, every flip flop expresses a rather randomized behavior, if the timing of the start and stop signals is close to the required setup and hold times.

For the following reasons, this process is not only time consuming but also very error prone: the line stretcher has to be adjusted in steps of 1 mm or below, which is but easy; for every length, at least 100 samples have to be taken in order to achieve a suitable statistic. Also, all external components, such as the signal generator, external wires and signal splitter have a negative impact on the precision of the calibration process. Furthermore, the entire process might be tainted due to thermal on-chip processes, which are not under control of the calibration process.

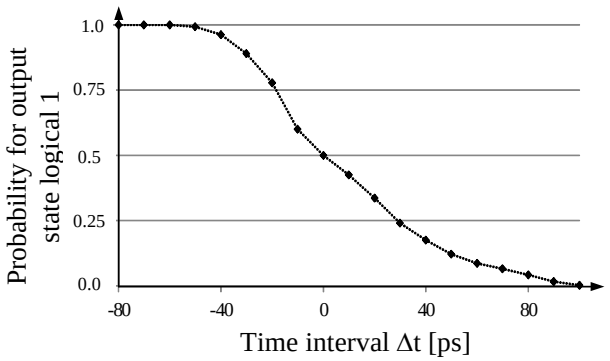

Fig. 5. Output probability for one single BOUNCE element, caused by calibration side effects and internal behavior of the flip flop.

As can be seen in Fig. 5, these aspects in combination with the timing of every flip flop lead to a specific output probability curve for every single BOUNCE element, depending on the time interval Δt. The depicted element exhibits a 50 percent output probability for a delay $\Delta t=0$ ps. If the time interval increases, the output probability decreases and vice versa. However, for multiple delay measurements, this behavior can be compensated, since the results rely to this switching probability. For example: if the BOUNCE element, shown in Fig. 5, provides a logical 1 in half of all measurements, the input time delay can be calculated to $\Delta t=0$ ps. But, BOUNCE is also designed to measure single events, where multiple measurements cannot be done. Thus, it is of particular interest to narrow the delay range of changing output probabilities as much as possible to increase the precision of a single output.

The remainder of this paper proposes an improved calibration process that is easy to perform and that yields accurate results.

IV. Hybrid Approach to Optimize Calibration

This section describes a hybrid approach in which BOUNCE is augmented with another asynchronous system, called X-ORCA [6][8]. X-ORCA is a descendent of BOUNCE that is easy to calibrate and tailored to the measurement of the phase difference of two incoming *periodic* signals. This system is further described in Subsection IV.A. Afterwards, Subsection IV.B focuses on the hybrid of both, BOUNCE and X-ORCA, and discusses how an accurate calibration can be performed.

A. X-ORCA: A High-Resolution Phase-Shift Detector

X-ORCA has the very same top-level layout as BOUNCE has. But rather than using simple flip flops, X-ORCA employs multiple instances of individual phase detectors. Such a phase detector is shown in Fig. 6, and consists of an XOR gate and a subsequent binary counter. The XOR gate processes the two periodic signals, and indicates whether the two signals differ from each other or not. Since the XOR gate is connected to the enable input of a partner counter, a logical 1 on its output

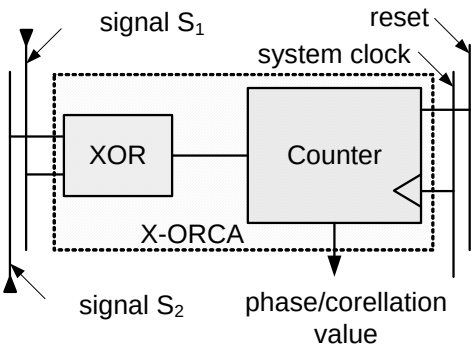

Fig. 6. Schematic of the original X-ORCA phase detector.

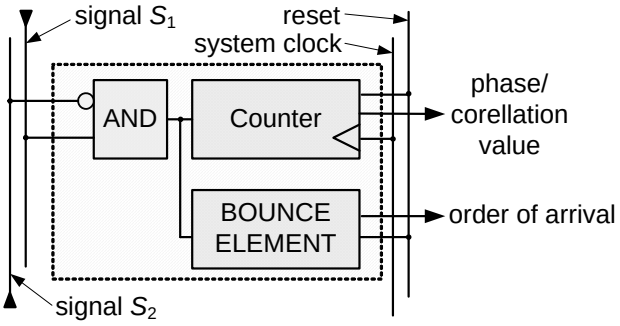

Fig. 7. Schematic of the combined X-ORCA/BOUNCE element. Notice the modified signal entry gate.

allows the clock signal to increase the counter value. After a reasonably long period of time, the counter value gives a fair estimate of the phase shift as long as the clock signal is uncorrelated with the two periodic input signals. Actually, the phase shift is determined by the quotient of the counter value and the number of clock cycles as well as the frequency of the two incoming signals.

Since the distribution of the phase detectors is similar to the distribution of the flip flops in BOUNCE, every phase detector observes its individual phase shift, even though the two input signals do not change their phase to each other. Furthermore, since all these phase detectors operate in parallel, they allow for averaging and interpolation, which yields way better results than the (counter's) clock frequency would suggest. A first prototype [9] on an Altera CycloneII FPGA yields a resolution of 20 ps for input signals of up to 300 MHz, even though a clock frequency of only 85 MHz was used.

B. Combining BOUNCE and X-ORCA

Combining BOUNCE and X-ORCA is technically rather simple. Since both systems are connected to a pair of signal wires, X-ORCA elements can easily be placed among BOUNCE elements. In so doing, the internal structure of both elements has to be changed slightly. However, these changes do not affect the aforementioned general behavior of both systems. Fig. 7 shows an illustration of the hybrid implementation for one element.

As can be seen, the former XOR gate has been replaced by an AND gate with one inverted input port. This gate generates a pulse with a pulse width according to the phase shift of both signals S_1 and S_2. Keep in mind that the XOR gates produced two pulses per signal cycle, one between the rising edges as well as one between the falling edges. On the other hand, the utilized AND gate generates only one pulse, either on the rising edges or the falling edges of both signals. This ensures the operation of both, the counter and the BOUNCE element. The counter determines the phase shift value of S_1 and S_2. The BOUNCE element is designed to operate only on the falling edges of S_1 and S_2. Given that signal S_2 arrives ahead of signal S_1, the pulse (generated by the modified AND-gate) occurs at the falling edges of S_1 and S_2. The BOUNCE element detects this pulse and sets its output value to a logical 1. No pulse occurs between the falling edges of both signals if signal S_1 arrives first. The BOUNCE element keeps a logical 0 at its output. Thus, the BOUNCE element detects whether a positive or negative phase shift exist, i.e., which one of the signals arrived first.

Obviously, the phase shift information obtained from the counter is rather useless, if only the single BOUNCE element is considered. But as already shown in [5], the complete BOUNCE architecture consists of up to hundreds of those detectors. The major contribution of the counter is that it provides a virtual time base for the entire system. It enables the system to combine a certain output vector of all BOUNCE elements with a precisely determined timing value obtained from the phase shift value generated by that counter.

As already described in Section III, this combination of time (or delay) values to BOUNCE' output vectors is the main task during calibration. Furthermore, the combined approach supersedes the requirement for external calibration signals. These external signals were necessary since the precise timing information of on-chip-generated signals was not available without X-ORCA.

The next section provides detailed description of the experimental setup used to evaluate this approach. The results are provided in Section VI.

V. METHODS

For all experiments, an Altera DE2-70 FPGA development board [10] was used. This development board features a CycloneII FPGA with 70k of programmable logic elements. The implemented BOUNCE system utilized a rather limited number of only 37 detectors. For evaluation purposes, every BOUNCE detector was equipped with an additional counter, forming a structure as already shown in Fig. 7.

These elements were spatially distributed within one single row of 37 logic array blocks (LAB). In every LAB, one dedicated logic element was used to integrate the modified AND-gate. Another dedicated logic element acts as the detector flip flop. The hardware resources for the counters reside next to the detectors. The counter hardware is considered noncritical since it is clocked at a rather low clock rate of only 50 MHz.

The on-board oscillator of the DE2-70 board provides a highly stable 28.63636 MHz rectangular signal as the signal source for both signals S_1 and S_2. However, calibration still requires different delays Δt. In order to provide different, fine-grained delays, the combined approach also includes a configurable delay line for the incoming signals S_1 and S_2. These delay chains were built by 64 logic elements each. Every logic element provides a propagation delay of approximately 70 ps since the very fast carry path is used to connect the logic elements. Thus, the delays can vary between 0 ns and 4.5 ns per signal. Since the exact propagation delays vary among the logic elements, a total 64*64 different delay values can be configured and applied to the calibration process of BOUNCE. For the calibration method described in this paper, 400 different delays were used, ranging from approximately –4.5 ns to -2.0 ns. During the experiments, the system performed one hundred single shot measurements per delay value.

VI. Results

As a first result, Fig. 8 shows the timing behavior of the systems 37 BOUNCE elements for different delay values ranging from -4.5 ns to -2.5 ns. As can be seen, these elements exhibit an output value change at different points in time. Every BOUNCE element shows an output value of logical 1 for every measurement, until a certain delay value is reached. The elements characteristic delay value is determined mainly by the geometrical position on the chip as well as the automatically synthesized signal routing. If the delay is increased beyond that characteristic value, the element provides outputs of logical 0. A main indicator for the precision of the BOUNCE elements is the time interval during which both output values occur, i.e., the time duration during which a BOUNCE element indeed exhibits a randomized behavior. Here, Fig. 8 indicates, that the considered BOUNCE elements exhibit a rather crisp timing behavior. The old calibration approach lead to an average range of uncertainty (or transition area) of approximately 170 ps, shown in Fig. 5. Using the new calibration approach, every single BOUNCE elements provides absolutely stable output values except during a rather short transition range of less than 20 ps. To prove this indication, Fig. 9 shows a graph, where all the 37 BOUNCE elements were merged to a virtual point in time. The arbitrary origin is defined as that point in time where the output probability of a logical 1 drops below 50%. That neutral point is calculated for all BOUNCE elements and the elements' timing behavior is condensed to that point.

As a result, the precision of the new calibration approach can be considered to be more than five times better than that of the old approach. Furthermore, the results indicate, that most of the uncertainty seems to come from the laboratory equipment used during the old approach. The new approach allows for abandon most of the external gear, except for the oscillator; all other required components can be realized by on-chip ressources. In so doing, most error sources were eliminated.

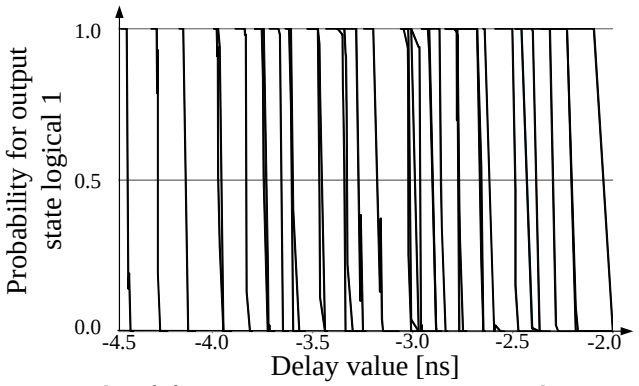

Fig. 8. Results of first experiment, every curve corresponds to one BOUNCE element. Every single element changes its output value at a certain delay.

VII. Discussion

This paper has presented some detailed characteristics of the BOUNCE time interval measurement system. It was examined that the classic calibration approach for BOUNCE is prone to errors and uncertainties. In turn, these aspects also affect the reliability of BOUNCE' results gained during measurements of unknown time delays Δt. During multiple measurements the influence of calibration errors can be reduced by statistical analysis. However, especially during single event measurements, statistical analysis is unavailable. Thus, calibration errors lead to a significant uncertainty of a single-shot measurement.

To overcome this limitation, this paper has presented a new calibration approach, utilizing an additional phase shift detector, known from the X-ORCA architecture. This phase shift detector allows for the use of highly stable on-chip signals for calibration, since X-ORCA is able to calculate a high-precision phase shift. The phase shift can be easily transferred into a time value. This time value provides the timing information, necessary for the calibration of BOUNCE.

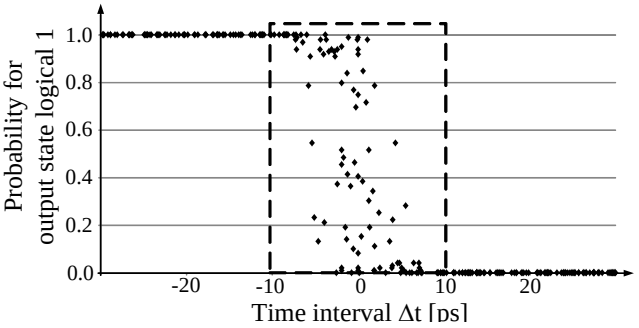

Fig. 9. Illustration of transient area of all BOUNCE elements. All elements fully change their output behavior within 20 ps (dashed line).

As a result, a prototypical implementation of the combined calibration approach on an Altera CycloneII FPGA provides a proof-of-concept. Due to the fact, that external system components as well as human intervention are no longer required during calibration, the precision of BOUNCE has been improved by a factor of five.

Obviously, the presented system with its 37 BOUNCE elements exhibits only limited resolution. As can be seen in Fig. 8, resolution varies between approximately 100 ps and 200 ps. However, according to [4], the resolution can be easily improved by adding more BOUNCE elements to the system. Combining the improved calibration accuracy with recent research results [4][5] enables BOUNCE for time measurements at high resolution and high precision. This also holds for single-shot measurements.

These results are particularly useful in the domain of indoor-localization, especially when small and mobile devices are required. Due to its internal structure, BOUNCE can be implemented in off-the-shelf components, such as FPGAs. Thus, further research will be dedicated to the use of BOUNCE in low-cost indoor localization systems. Here, the detection of real-world radio signals and their timing behavior is of particular interest.

As a second field of interest, high-precision on-chip timing evaluation is in focus of further research efforts. Since the combined BOUNCE/XORCA approach has provided precision of better than 20 ps, this allows for the investigation of the timing of different on-chip components. These components range from simple logic elements to input and output connections of the FPGA and, of particular interest, the timing of signal routing structures within the FPGA.

ACKNOWLEDGMENTS

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REFERENCES

[1] Jinhong Wang, Shubin Liu, Lei Zhao Xueye Hu, and Qi An, “The 10-ps Multitime Measurements Averaging TDC Implemented in an FPGA”, *IEEE Trans. Nucl. Science*, vol. 58, no. 4, pp. 2011–2018, August 2011.

[2] Kalisz, J., “Review of Methods for Time Interval Measurements with Picosecond Resolution”, *Metrologia*, vol. 41, no. 1, pp.17-32, 2004.

[3] Claudio Favi, Edoardo Charbon,”A 17ps Time-to-Digital Converter Implemented in 65nm FPGA Technology”, *17th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2009), pp. 113-120, February 2009*

[4] Ralf Salomon, Ralf Salomon, “BOUNCE: A new High-esolution Time-Interval Measurment Architecture”, *IEEE Embedded Systems Letters (ESL)*, vol. 1, no. 2, pp. 55-59,August 2009

[5] Ralf Joost, Ralf Salomon, “BOUNCE: A Concept to Measure Picosecond Time Intervals with Standard Hardware”, *13th IEEE International Conference on Emerging Technologies and Factory Automation (ETFA)*, pp. 1010-1015, September 2008

[6] Mathias Hinkfoth, “X-ORCA: FPGA-Based Wireless Localization in the Sub-Millimeter Range”, *20th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2012)*, pp. 29-32, Februar 2012

[7] Microlab, “Line Stretchers, SR Series”, 2008.

[8] Enrico Heinrich, Ralf Joost, Marian Lüder, Ralf Salomon, “Precise Indoor Localization with Low-Cost Field-Programmable Gate Arrays”, *IEEE Symposium Series on Computational Intelligence (SSCI 2011)*, pp. 23 - 28, April 2011

[9] Enrico Heinrich, Marian Lüder, Ralf Joost, Ralf Salomon, “X-ORCA – A Biologically Inspired Low-Cost Localization System”, *10th International Conference on Adaptive and Natural Computing Algorithms*, pp. 373-382, April 2011

[10] Terasic Technologies Inc.,”Altera DE2-70 User Manual”, 2009