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The Trigger-Time-Event-System for Wendelstein 7-X: Overview and First Operational Experiences

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Abstract—**The superconducting stellarator Wendelstein 7-X (W7-X) started plasma operation in December 2015 after the commissioning phase of the machine. The main technical and diagnostic systems have been finished successfully. The timing system is an important part of the Control, Data Acquisition and Communication systems of W7-X.**
The first version of the TTE-system is in routine operation at the W7-X experiment. Since 2004 it has been used for the commissioning of the control and data acquisition components, and also for the stellarator WEGA.
The commission of the second version of the TTE-system is still on going and planned to be finished end of 2016.
Starting with an introduction of the TTE-system of W7-X, this contribution describes the main features of the TTE-system. The actual state of the TTE-system and the network topology will be presented. Finally, first experiences of W7-X operational phase OP1.1 related to the TTE-system are discussed.

Index Terms—**Control and data acquisition, FPGA device, timing system, synchronization, trigger-time-event functions,**

I. Introduction

THE stellarator Wendelstein 7-X (W7-X) is designed for stationary operation [1]. Its superconducting magnet system, which consists of 50 planar and 20 non-planar coils, produces an optimized magnet field. For the heating of the plasma three heating systems: ECRH, NBI and ICRH are foreseen. Especially, the ECRH is capable of producing stationary heating power with high power.
The main goal of W7-X is to demonstrate the potential of an optimized stellarator for a fusion reactor.
High performance fusion plasmas in a stationary operation can only be achieved, if an intelligent control system sets up and supervises all plasma parameters to be in necessary parameter range [2].

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The central control system of W7-X consists of the following parts safety control, operational management, real time control for plasma experiments, and Trigger-Time-Event-System (TTE system). The TTE system fulfills important tasks for synchronization of control sequences and the measurements of technical and plasma physical data acquisition systems [3], [4], [5].
The commissioning of W7-X was finished at the beginning of December 2015. The first plasma discharge in Helium was performed during the first operational phase OP1.1 on 10th of December 2015. Another highlight of OP1.1 was the first plasma operation in Hydrogen at the beginning of February 2016. In OP1.1 940 experiment programs were performed, which served for technical tests, conditioning of the plasma vessel, and for plasma-physical research.
After a description of the structure and functions of the TTE system, the realized status of the TTE systems will be described. The operational experiences during OP1.1 will be discussed. A short outlook for the preparation of TTE system for the next operational phase OP1.2 will be given.
This contribution ends with a short summary.

II. Requirements of the Tte System

For development of the TTE system a number of requirements have been defined. The following important requirements for the whole TTE system have to be considered during development process of the TTE system and its subsystems:

- The TTE system must be operable and reliable during the long operational time of W7-X (approx.: 20 years).
- The TTE system has to be scalable. The number of devices of the TTE system should not be limited in principle.
- The TTE system must be available in the whole experimental area of W7-X.
- The hardware of different parts of the TTE system should be selected in a way that an enhancement during the life time is possible.
- The TTE system must provide a common time base for all control and data acquisition components of W7-X with sufficient time accuracy in a range of some ns.

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- A time synchronization of industrial control PCs and Programmable Logic Controllers (PLCs) has to be supported, as well.
- The system must provide time capturing functions for data acquisition purposes as well as functions for producing trigger signal sequences and clock signals.
- The system must be able to distribute and process of event messages.
- The implementation of all TTE functions into the technical components and diagnostics should be easy.

III. The Architecture of TTE System

The TTE system is an independent subsystem of the overall control and data acquisition system of W7-X. It consists of the main components central TTE system, local TTE systems as a part of the technical components, diagnostics, and the TTE network. Fig. 1 shows the structure of the TTE system.

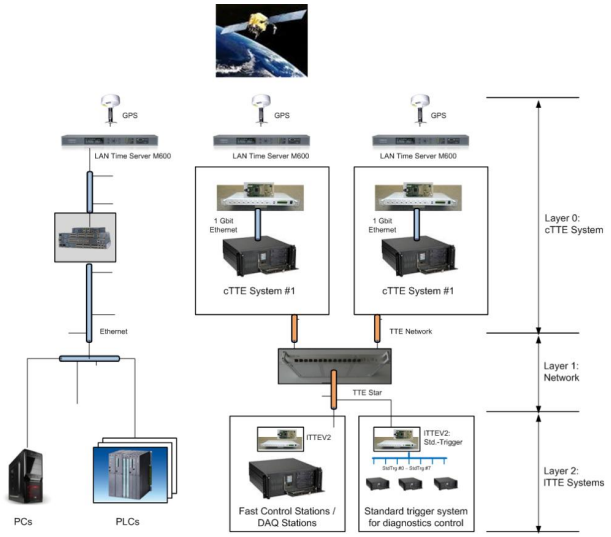

Fig. 1. Structure of TTE system.

The TTE system has a hierarchical structure with the central TTE system (cTTE system) on the top (layer 0). An arbitrary number of local TTE systems (lTTE systems) define the layer 2 of this structure. The TTE network connects all components of layer 2 with the cTTE system.
All important components of the TTE system are described in Table. 1.

TABLE I
DESCRIPTION OF MAIN COMPONENTS OF TTE SYSTEMS

Main system	Subsystem	Function/Properties
cTTE System	2x cTTEV1/V2 card with control PC	64 Bit time counter as W7-X time basis, Synchronization of W7-X time counter value with utc standard time, Transmission of event messages requested by the fast sequence controller (experiment program control), Measurement of transmission delay of the data transfer via TTE network (will be available with cTTEV2 version).
	3x LAN Time Server: ML600	Providing a very stable clock for synchronization of the cTTEV1/V2 card osciallator, Provide UTC time information for synchronization of the cTTE time counter with UTC time,
TTE network	TTE-Star V1/V2, fiber network	Unidirectional data transmission (TTE devices of version 1) or bidirectional data transmission (TTE devices version 2) between cTTE system and lTTE systems. Transfer of synchronization signals, time information, and event information.
	IRIG-B converter	Conversion of time packet information into the IRIG-B time protocol format for devices using IRIG-B Interfaces.
lTTE System	lTTEV1/V2 device with control PC	64 Bit time counter for the local time. Provide hardware for following functions: Send and receive trigger signals, pulse- and pulse sequence generators, delay functions, impulse counter functions, time capture functions, event processing,
Normal Ethernet	Interface between control-PC and c/lTTEV2 devices	Configuration and control of l/cTTEV2 devices, Read-out of status and interrupt information, and register values of the TTE devices,
Standard trigger system (sTS)	Experiment sequence controller, cTTEV1/V2 devices, TTE-network with TTE-Star devices, lTTEV2-StdTrg devices	lTTEV2-StdTr devices are preconfigured and operate without control PC. They receive and transfer 7 event messages as standard triggers, Synchronization of triggered diagnostics to the experiment sequence,

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IV. Hardware Realization

This section focuses on the implementation of all TTE-devices: cTTE card, lTTE card, lTTEV2-sTS, TTE-Switch and IRIG-B converter. The main design goals were the creation of a flexible, customizable implementation and the use of existing modules if possible:

- The existing TTEv1 system should be reused in the design process of the new TTEv2 devices [7].
- Especially, the internal connection structures for configuration and status should be utilized.
- Existing sub modules (I/O-Trigger, Alarm Timer, Time Capture …) should be updated. Known bugs shall be removed and the sub modules reused as far as possible.
- The integration of newly developed modules into the existing system should be made as comfortable as possible for the FPGA software developer.

A. Hardware Platforms of Prototypes and Final Devices

We used three different hardware platforms within the TTE-System. The cTTEv2 Card, lTTEv2 Card and the Std-Trigger-Card are implemented as prototypes on the ML605 Board [8] that is equipped with a Virtex 6 FPGA. The lTTEv2 card and the lTTEV2-sTS card use completely the same hardware. They only differ in the HDL code. For the final devices these designs are ported to a custom Printed Circuit Board (PCB) equipped with a Virtex 6 FPGA (XC6VLX130T) [9]. These motherboards are extended with different daughter boards. The cTTEv2 and the lTTEv2 card have different daughter boards as they have different I/O Ports. The TTE-Switch as well as the IRIG-B Converter are implemented on the Atlys Spartan 6 board [10].

B. Resource Utilization

As we implemented all designs on the final hardware and some designs also on prototype boards, we can state the resource utilization on all platforms. Table II gives an overview. For every design the number of used registers as well as the number of used Look up Tables (LUTs) is stated and the utilization in percent is shown in brackets.

Regarding the TTE-Switch as well as the IRIG-B design the resource utilization are not critical. We do not need many of these devices and the Atlys board is relatively cheap. Moreover, the resource utilization of the cTTE card is low. Furthermore, this device is used only twice (redundancy). Instead, the resource utilization of the lTTE device was critical during the implementation. This design should be the most flexible one utilizing the as many sub-modules as possible in the TTE-core. Moreover, the lTTE card is used at many measurement points distributed within the W-7X experiment. Hence, we used the relative small Virtex-6-130T with 130 thousand logic elements, which is cheaper than the Virtex-6-240T with 240 thousand logic elements. Actually, the resource utilization of 74% of the LUTs is close to the maximum. For more than 70% resource utilization the synthesis can be critical which may lead to suboptimal results.

TABLE II
OVERVIEW OF RESOURCE UTILIZATION

Type	Registers	LUTs	FPGA
cTTECard	13k (8%)	13k (17%)	Virtex6-130T
lTTECard	39k (24%)	59k (74%)	Virtex6-130T
StdTrigCard	29k (18%)	41k (52%)	Virtex6-130T
TTE-Switch	7k (12%)	5k (16%)	Spartan6-X45
IRIG-B	4k (7%)	7k (27%)	Spartan6-X45

C. Automation Enhanced Design Method

For the implementation of the cTTE card, we developed a novel approach to design complex HDL (Hadware description language) systems. Our approach faces the following general design problems:

- A bus interface connects a high number of submodules in the top-level module. There are different types of submodules (e.g., Counter, Interrupt manager, Timer, …) and different numbers of instances per type (e.g., 4 Counters, 1 Interrupt managers, 8 Timers, …).
- One Design goal is to use the given address space in an optimal way. If can reduce the bits to address the same amount of submodules, we save chip area and energy.
- It should be easy to add new submodule types to an existing system or to substitute existing types as well as to change the number of used instances per submodule type.

We assume that the specification provides the following information:

- The name of every submodule type.
- The number of instances of every type used in the system.
- The address width to address the internal registers for every submodule type.
- The number of interrupts per instance for every submodule type.

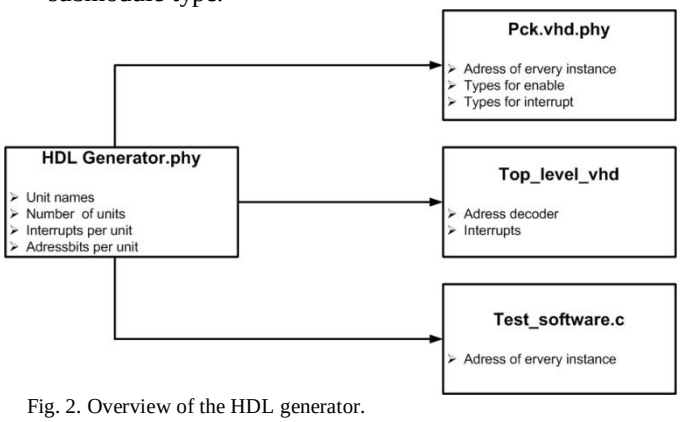

Fig. 2. Overview of the HDL generator.

To face the stated problems under the stated assumptions, we developed a python program that massively accelerates the design process. Figure 2 shows an overview of the program including the output files. The program does the following:

1. Generation of the address of every instance of every submodule type as a VHDL constant in a VHDL package. It would be possible to use the calculated addresses to

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generate a verification software as well as the address tables for the documentation.

2. Generation of an address decoder in VHDL that is capable of handling variable address widths. As an example, if instances of type A need 3 bits to address internal registers, the address decoder ignores the 3 LSBs of the address when addressing the instance. Instead, these 3 LSBs are used for addressing the internal registers of the instance. Thus, the decision whether a bit is used to address the instance of internal registers of an instance has to be done for every submodule type separately. Nevertheless, we have to state that all if-statements created by the python program for the address decoder are executed in a concurrent way and did not lead to timing penalties.
3. Generation of all interrupt assignments in VHDL.

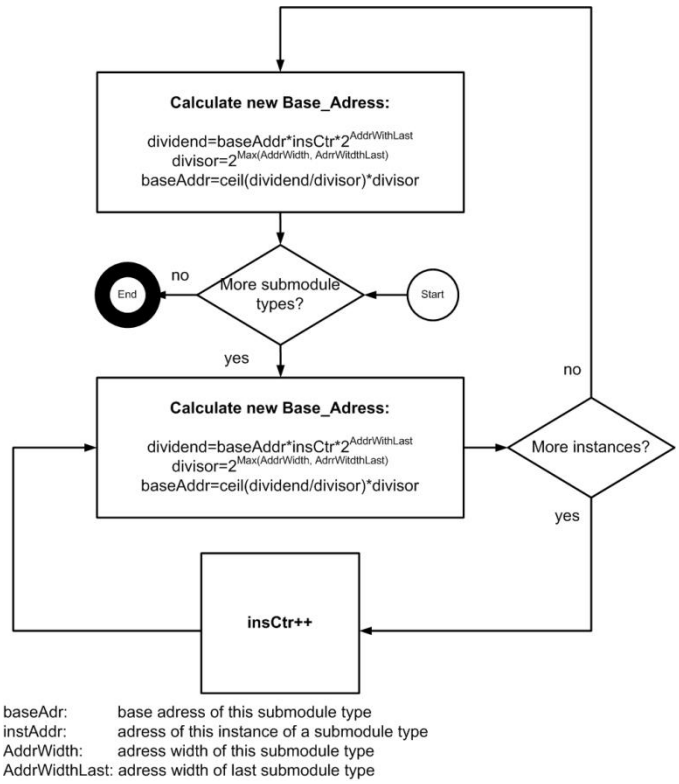

Fig. 3. Diagram of algorithm for address calculation.

Figure 3exhibits the algorithm used to calculate the address of every instance. The benefits of the proposed workflow is that it presents a generic way to accelerate the design of complex systems. It is easy to add new submodule types, to replace existing ones and to change the number of instances per type using the python script. Furthermore, the generated HDL code is easy to modify and maintain as the HDL code states all relevant information as constants. It is also possible to develop the same generic addressing scheme shown in Fig. utilizing VHDL Functions. Nevertheless, using an external program to create VHDL constants leads to a code that is much easier to read and maintain providing the same flexibility. Besides, the workflow accelerates the error prone work of writing VHDL constants for the address of every instance and the development of with-flexible decoders.

V. Software

Controlling the TTE boards requires a driver. The common TTE device driver software is usable for both local and central TTE devices. Because TTEV2 devices connect to their host via Ethernet all supported operating systems (VxWorks, Linux and Windows) use the same driver build on top of the network stacks of the operating systems.

The driver supports direct register access as well as a more easy-to-use application programming interface (API) called *TimeLib*.

The driver is complemented by usage examples and a wide set of unit and regression tests.

The usage of unit tests helped us to fix several bugs during hardware and driver development.

VI. Realization for OP1.1

The lTTE system for the technical components and diagnostics and the TTE network have been set up during the commissioning phase of W7-X.

The TTE system was already in operation since 2005. It was used for the tests of components and for the WEGA stellarator, which had been used as a testbed of the W7-X control system [6].

Before starting OP1.1 the ten years old GPS receivers failed and were replaced by three LAN time server ML600 (Meinberg).

Every technical component and diagnostic working during OP1.1 have been equipped with an lTTE system. All PLCs and PCs of the experiment and also all office PCs and network devices are synchronized with the LAN time servers by using the NTP protocol.

To fulfill higher demands for the time synchronization, the user has to integrate lTTEV1/2 devices into the control system of components. About 60 lTTEV1/2 devices are in usage for OP1.1.

The TTE network has been planned and set up along with the Ethernet network of a component. The cable type of the TTE network is a 50/125 multimode fiber. The TTE network has a tree structure with network nodes in the experiment hall and adjacent buildings and laboratories. At the moment about 20 TTE network nodes are installed.

The TTE network is not only available in the experiment area. It is also connectable in many laboratories for test purposes.

VII. Modification of the TTE System

In the course of the TTE project a number of new requirements for the TTE project have arisen. These new requirements can be divided into two categories: user driven changes and hardware based changes of requirement. Some of the users needed more TTE hardware devices as planned. Furthermore, the designer of diagnostics asked for TTE devices with new functionalities, e.g. time capture devices

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combined with a large FIFO or programmable pulse sequence generators. This kind of requirement has been considered by designing the new lTTEV2 card.

A very important extension of the capabilities of the TTE system was the introduction of a standard trigger system (sTS). The sTS distributes 7 different standard trigger signals within the whole experiment area. By using these triggers all triggerable diagnostics delivered in context of collaboration can by synchronized during a discharge. Each standard trigger is generated as a TTE event message by the cTTE System. The time of issue is requested by the experiment control system. The lTTEV2-sTS devices receive these event messages and generate a low voltage Transistor-Transistor-Logic **(**LVTTL) output with each trigger event. The lTTEV2-sTS version is realized as a pre-configured version of the standard FPGA image. It operates as a standalone device without a control host computer. Fig. 4 shows the first version of the standard trigger scheme for OP1.1.

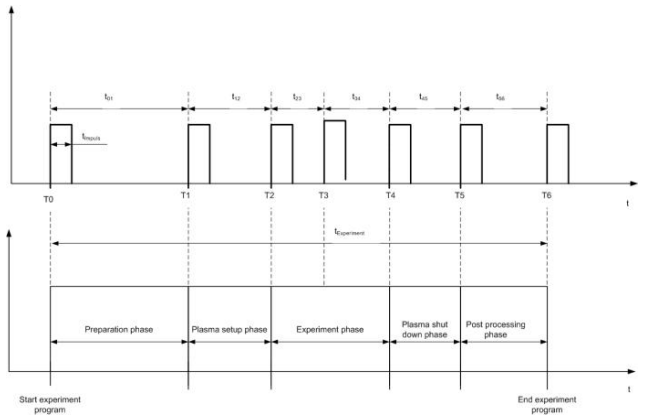

Fig. 4. Scheme of the standard trigger for OP1.1.

Furthermore, many changes of requirements for the TTE system are related by hardware reasons. Many ICs are no longer available and this demands a new hardware design. The more powerfull FPGA Virtex 6 (Xilinx) used for the c/lTTEV2 devices replaces the older Virtex 1000 FPGA (Xilinx). Due to the performance of Virtex 6 FPGA it was possible to add new properties of established TTE devices of the c/lTTE devices and also new devices were introduced. A flexible pulse sequence generator allows to program complex trigger schemes. Buffered time captures and time captures for periodic signals support high speed data acquisition systems. The PCI Interface of the c/lTTEV1 devices has been replaced by a 1 Gbit Ethernet interface. This enables the application in a variety of hardware platforms and as stand-alone devices It very much eases driver development too.

VIII. Experiences of OP1.1

The whole TTE system worked reliably with high availability during OP1.1. Only a few failures due to bugs in the FPGA and the driver code of single lTTE systems were detected. All bugs have been fixed meanwhile. During OP1.1 a work around could be found so that the operation of W7-X was not really affected.

During the operation within 10 years prior to OP1.1 we experienced degradation of the TTE network and the network receivers of the lTTEV1 card. Reasons for degradation and failures has been a contamination of fiber optic interfaces and / or an aging of the transceiver ICs. Therefore, the design of the c/lTTV2 devices utilized a new type of the transceiver ICs offering a larger amount of transmission power and more sensitivity on the receiver part.

IX. Next Steps

After shutting down the machine W7-X at the end of OP1.1, the preparation of new diagnostics for the next operation phase called OP1.2 has been started. A set of 80 new lTTEV2 devices will be purchased.

The planning of the extensions of the TTE network is running. New lTTE systems have to be connected to the TTE network and the communication between cTTE system and the lTTE systems will be set up as a bi-directional communication channel.

The development of the hardware of the new cTTEV2 device has to be finished.

The scheme of the standard trigger will be update in order to fulfill the requirements of the plasma discharges in OP1.2.

Finally the properties of the system synchronization must be measured for every local TTE system. This allows an individual compensation of the transmission delay of the time packets via the TTE network for every lTTEV2 receiver. This measure leads to a better time value synchronization of the lTTE system time counter values.

X. Summary

The fusion experiment W7-X has successfully accomplished the commissioning and the first operational phase OP1.1.

The TTE system is an important part of the control and data acquisition system of W7-X.

All requested TTE system requirements for OP1.1 have been fulfilled. The TTE system works with high reliability and availability.

In preparation of the upcoming W7-X operational phase OP1.2 the TTE system has to be extended for an integration of a large number of new diagnostics.

Furthermore, new versions of TTE hardware will be developed and will be integrated into the TTE system, e.g. the second version of cTTE device, and the TTE network switch device TTE-Star.

Another important OP1.2 working package is the measurement of individual transmission delays between transmitters of cTTE and lTTE systems. The extended properties of the cTTEV2 devices and the TTE network devices TTE-StarV2 provide an integrated transmission delay measurement. The measured transmission delay values will be used for a compensation of transmission delays. This enables a better time value synchronization of the lTTE system time counter devices.

The installation of a central monitoring system for all types of TTE hardware devices is useful for collecting and assessing of TTE system status information.

REFERENCES

[1] H.-S. Bosch, R. Brakel, M. Gasparotto et al., "Transition from Construction to Operation Phase of the Wendelstein 7-X Stellarator", IEEE Trans. on Plasma Science., vol. 42, no. 6, pp. 432-438, Feb. 2014.

[2] A. Werner, T. Bluhm, M. Grahl, J. Schacht et al., "Cutting edge concepts for control and data acquisition for Wendelstein 7-X", IEEE 25th Symposium on Fusion Energie (SOFE), 2013,

[3] J. Schacht, H. Niedermeyer, C. Wiencke, J. Hildebrandt, "A trigger-time-event system for the W7-X experiment", J. Fusion Eng. Des., vol. 60, issue3, June 2002.

[4] J. Schacht, H. Niedermeyer, H. Laqua, "Synchronization of processes in a distributed real time system exemplified by the control system of the fusion experiment WENDELSTEIN 7-X", Proceedings of the 14th IEEE-NPSS conference on Real time, 2005, pp. 43-48.

[5] J. Schacht, H. Niedermeyer, H. Laqua, "The Trigger-Time-Event System for the W7-X Experiment", Proceedings of the 12th IEEE Real Time Conference on nuclear and plasma science, Valencia, June 2001, pp. 240-244.

[6] J. Schacht, D. Aßmus, T. Bluhm, "Stellarator WEGA as a test-bed for WENDELSTEIN 7-X control system concepts", J. Fusion Engineering and Design, vol.83, issues 2-3, 2008, pp. 228-235.

[7] J. Schacht, J. Skodzik, CoDaC Team, "Multifunction-timing card lTTEV2 for CoDaC systems of Wendelstein 7-X", IEE Transactions on nuclear science, http://ieeexplore.ieee.org, digital object identifier 10.1109/TNS.2015.2425895.

[8] Virtex-6 FPGA ML605 Evaluation Kit. [Online] Available: http://www.xilinx.com/products/boards-and-kits/ek-v6-ml605-g.html.

[9] Virtex-6 Family Overview. [Online] Available: http://www.xilinx.com/support/documentation/data_sheets/ds150.pdf.

[10] Atlys Spartan-6 FPGA Trainer Board. [Online] Available: http://store.digilentinc.com/atlys-spartan-6-fpga-trainer-board-limited-time-see-nexys-video/.