PROTECTING CGRAS WITH THE HERA METHODOLOGY

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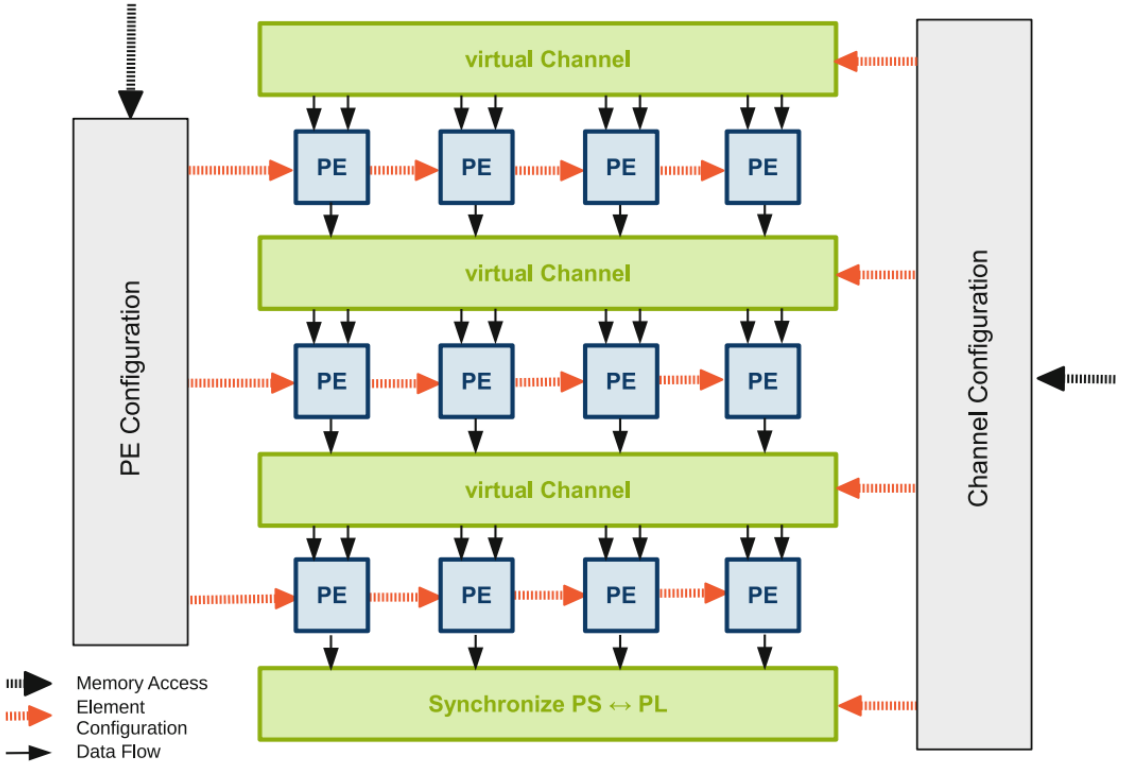
INTRODUCTION TO CGRAS

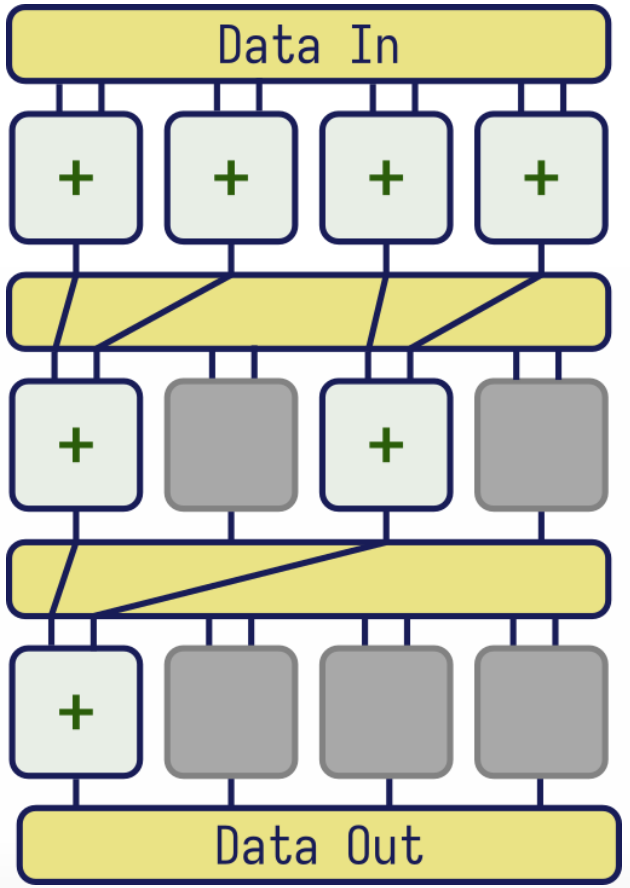
- CGRAs (Coarse-Grained Reconfigurable Arrays) are adaptable computing architectures
- Consist of programmable computation blocks and interconnects
- Offer flexibility and high performance for specific tasks



From: Fricke, F., Werner, A., Shahin, K., Huebner, M. (2018). CGRA Tool Flow for Fast Run-Time Reconfiguration. In: Voros, N., Huebner, M., Keramidas, G., Goehringer, D., Antonopoulos, C., Diniz, P. (eds) Applied Reconfigurable Computing. Architectures, Tools, and Applications. ARC 2018. Lecture Notes in Computer Science(), vol 10824. Springer, Cham. https://doi.org/10.1007/978-3-319-78890-6_53 (Used with Permission)

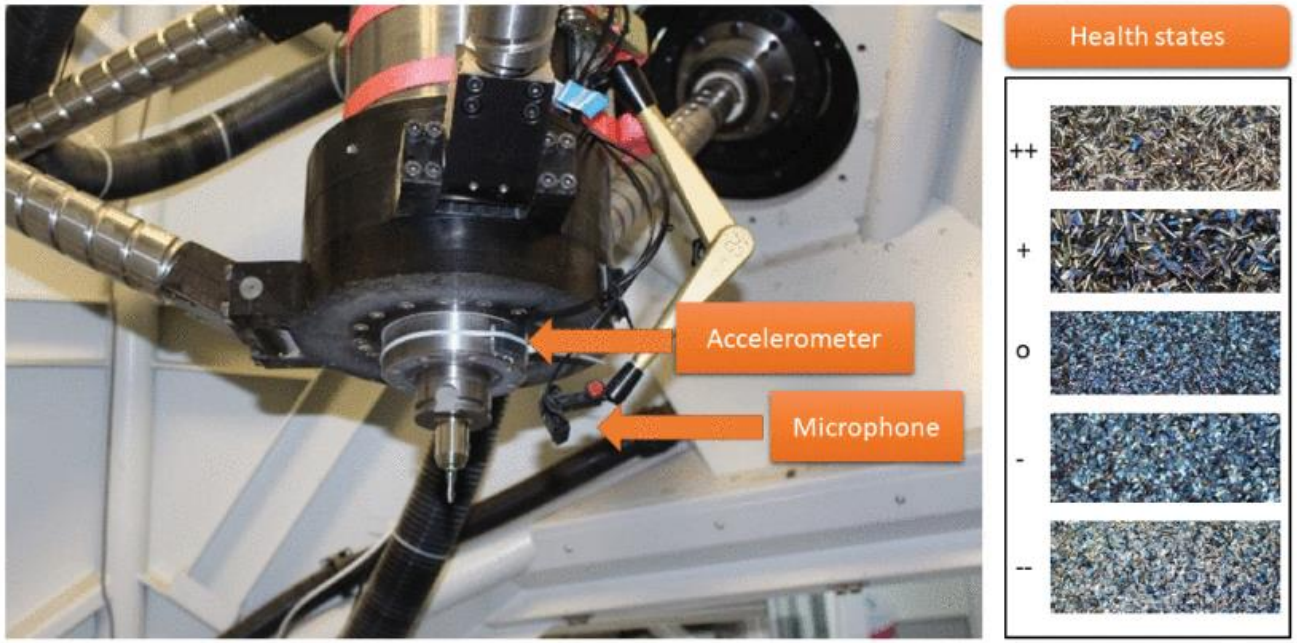
INTRODUCTION TO CGRA (CONT.)

- Enable dynamic hardware reconfiguration
  - Similar to FPGAs but with usually more dataflow oriented
- Ideal for parallel processing and complex computations
- Provide a balance between flexibility/programmability and efficiency



CGRAS IN INDUSTRY 4.0

- Industry 4.0 demands adaptable, high-performance computing
- CGRAs support real-time data analytics and machine learning
- Essential for smart manufacturing and IoT integration



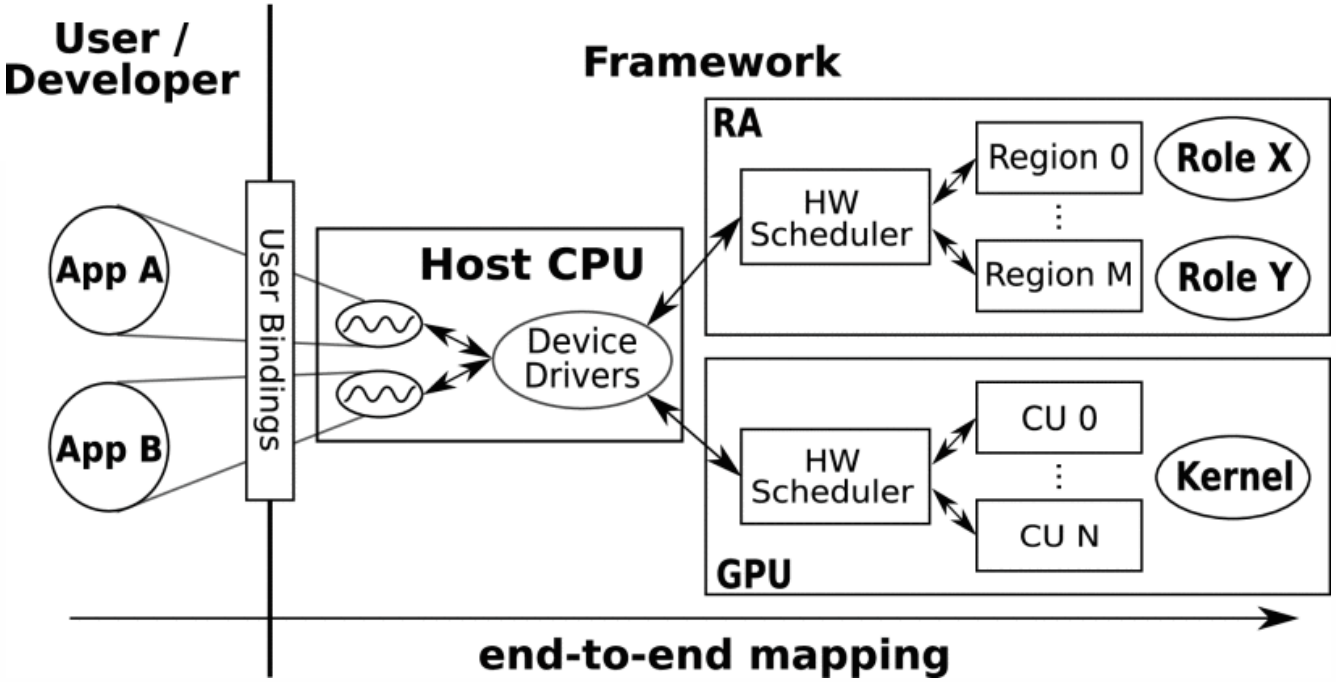
From: P. F. Suawa, A. Halbinger, M. Jongmanns and M. Reichenbach, "Noise-Robust Machine Learning Models for Predictive Maintenance Applications," in IEEE Sensors Journal, vol. 23, no. 13, pp. 15081-15092, 1 July, 2023, doi: 10.1109/JSEN.2023.3273458 (used with permission)

SECURITY CONCERNS IN INDUSTRY 4.0

- Security challenges similar to those faced by FPGAs
- Importance of module separation from different vendors
- Focus on robust security design in interconnected systems

THE HERA METHODOLOGY

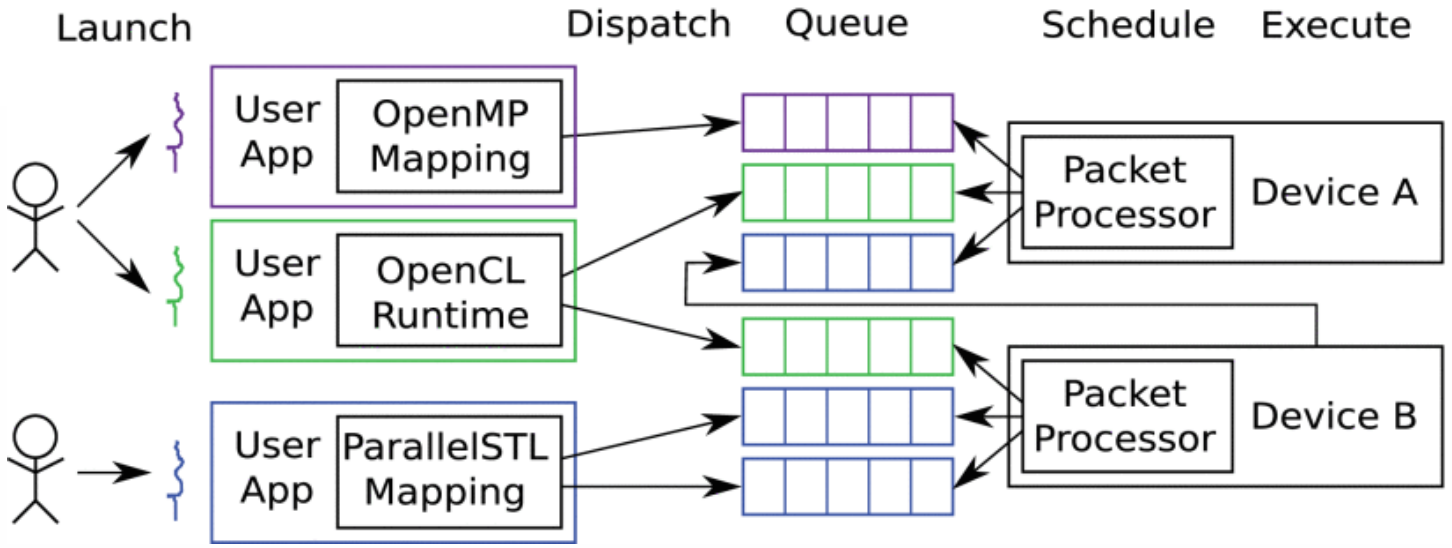
- HERA: Heterogeneous Reconfigurable Architectures
- Focuses on multi-user capabilities and accessibility
- Enhances security and efficiency in reconfigurable computing



From: P. Holzinger and M. Reichenbach, "The HERA Methodology: Reconfigurable Logic in General-Purpose Computing," in IEEE Access, vol. 9, pp. 147212-147236, 2021, doi: 10.1109/ACCESS.2021.3123874 (Used with permission)

PACKET PROCESSOR FOR CGRAS

- Responsible for task scheduling and dispatching
- Optimizes resource allocation and workload management
- Key component in managing CGRA's dynamic adaptability



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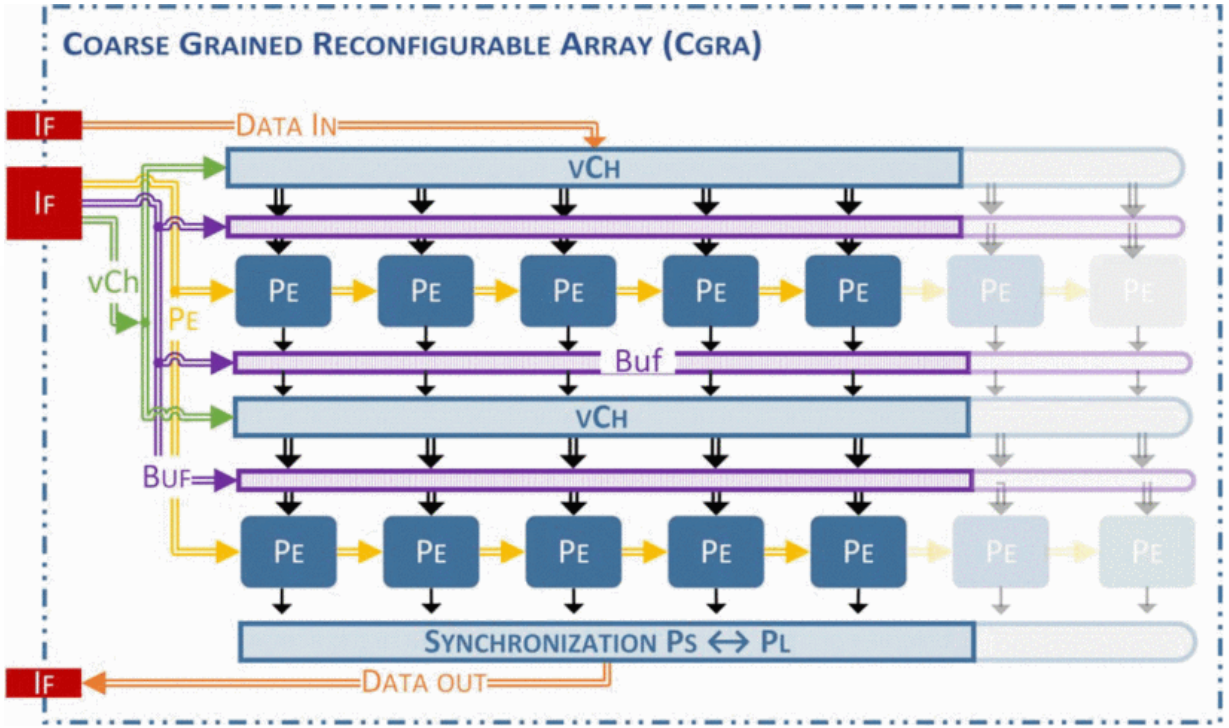
TARGET PLATFORM: VCGRA

- CGRA implemented as firmware on FPGAs
- Overlay architecture enhances flexibility and upgradability
- Allows for rapid prototyping and deployment of CGRA designs



From: F. Fricke, A. Werner, K. Shahin, F. Werner and M. Hübner, "Automatic Tool-Flow for Mapping Applications to an Application-Specific CGRA Architecture," *2019 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*, Rio de Janeiro, Brazil, 2019, pp. 147-154, doi: 10.1109/IPDPSW.2019.00033.
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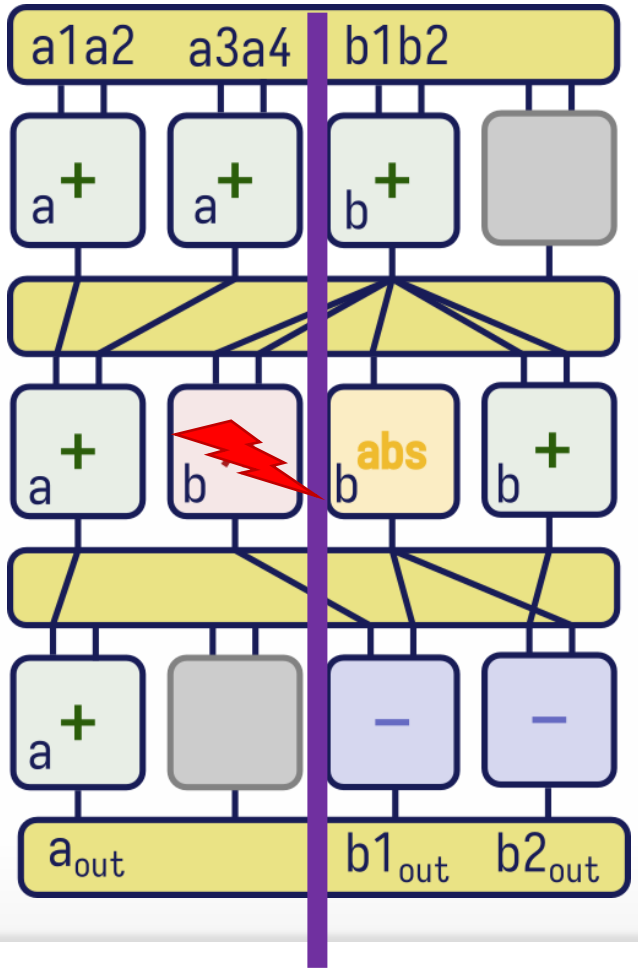
RESOURCE SHARING AND SECURITY IN CGRAS

- CGRAs should utilize resource sharing
- Main Issues:
  - Memory safety
  - Side Channels
- Pure Time Slicing or Partitioning not very efficient

►→ Consolidate Tasks

►→ New Side Channel



CONCLUSION

- CGRAs might play a role in Industry 4.0
- Security Aspects currently not thoroughly investigated yet
- HERA methodology can help