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New Developments for the Trigger-Time-Event System for the W7-X Experiment

J. Schacht, T. Brockmann, M. Marquardt, J. Recknagel, and T. Schröder

***Abstract*—Since the first plasma operation in 2015, the superconducting fusion experiment Wendelstein 7-X has successfully completed 4 experiment campaigns (OP1.1, OP1.2a, OP1.2b, and OP2.1). The machine maintenance phase was completed at the end of January 2024, followed by the commissioning of W7-X. The start of the scientific plasma operation phase OP2.2 is planned for September 2024.**

The Trigger Time Event (TTE) system is used by the central control systems, the technical components and the diagnostics of W7-X for their time synchronization, for processing events, and for generating and receiving trigger signals. This use cases makes it necessary to adapt the TTE system to the changing requirements of users.

After an introduction to the functions and structure of the TTE system, this contribution describes the current expansion status of the TTE system and the planned modifications and expansion of the hardware and software of the TTE system. Finally, the current status of the planned work on the TTE system for the upcoming W7-X operational phase OP2.2 is presented. The contribution ends with a summary.

***Index Terms*—Event distribution, synchronization, timing system, trigger generation,**

I. Introduction

THE Wendelstein 7-X fusion experiment is based on the stellarator principle and has a magnet system with 50 non-planar and 20 planar superconducting coils. Stationary plasma operation with full heating power is possible up to a maximum discharge duration of 30 minutes [1 - 4].

The first scientific plasma operation took place in December 2015. So far, 4 operational phases have been successfully completed, in which a total of 6,559 plasma discharges with a total plasma time of 473 min have been generated [5 - 8].

The next operational phase (OP2.2) will begin with scientific plasma operation in September 2024. Commissioning of the Wendelstein 7-X facility has been underway since the beginning of 2024 and the first plasma discharges will be carried out in June 2024 as part of the commissioning process.

The Wendelstein 7-X is a very complex technical system consisting of many technical installations (e.g. vacuum systems, cooling systems, magnetic field systems, plasma heaters [9 - 12]), fueling systems [13], as well as operational and scientific diagnostics [14 - 17] (diagnostics for measuring plasma energy, plasma density, turbulence measurements, i.a.).

During the preparation and execution of the plasma experiments, processes for control and data acquisition must be synchronized in the control and data acquisition systems themselves as well as between the systems. It should be possible to start certain control actions at predefined times. With multi-channel data acquisition, synchronous clock signals are often required for the A/D converters. Recorded events and measured values should be provided with a time stamp in order to evaluate event chains and measured values across systems.

Many fusion experiments and particle accelerators have developed their own trigger and timing systems (e.g. [18 - 22]) to meet their specific requirements in terms of synchronization, time accuracy and the generation and processing of triggers.

The trigger time event system (TTE system) developed specifically for the requirements of W7-X was put into operation before the start of the first W7-X operating phase OP1.1 in December 2015 [23]. Since then, the TTE system has been continuously expanded and technically enhanced.

This article introduces the key requirements and architecture of the TTE system. Important innovations for TTE system components are then described. This is followed by a project status of the TTE system. The article ends with a short summary and an outlook.

II. Requirements for the TTE System

The main requirement for time-related functions is the provision of a synchronized clock signal, which is derived from a central clock generator. The local time counters should be synchronized system-wide to a central clock. The requirements for the accuracy of the synchronization depend on the specific application. For example, a clock synchronization in the range of 10 ms - 50 ms is sufficient for a PLC application. For fast control tasks, this should be better than 1 ms. For data acquisition of high-frequency signals, a time resolution in the range of 100 ns - 1 µs is often required. Alarm functions with absolute and relative alarm times and time capture functions are also required.

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The analysis of the control and data acquisition requirements for W7-X for a timing system revealed that the system should also be able to process trigger signals and event messages. For the trigger functions, it should be possible to read in and output trigger signals via a signal interface. It should also be possible to generate periodic pulses and user-defined pulse sequences.

The TTE system should be expandable without limitation to enable the integration of new control and data acquisition systems into the TTE system.

The third category of requirements describes the ability to send and process special event messages within a system and between systems. Table I summarized the most important requirements for the TTE system.

TABLE I
IMPORTANT REQUIREMENTS FOR THE TTE SYSTEM

Topic	Requirement
TTE system structure	The number of TTE connected units must be flexible and not limited.
	The structure should be hierarchical: The cTTE system is at the top and the local TTE systems are at the lower level of the TTE system.
	The TTE system has to be scalable. The number of devices of the TTE system should not be limited in principle.
	The TTE system must be available in the whole experimental area of W7-X.
Reliability	The TTE system must be operable and reliable during the long operational time of W7-X (approx.: 25 years).
Time functions	The TTE system must provide a common time base for all control and data acquisition components of W7-X with a time increment of <= 20 ns.
	The clock for the central time counter device should have a low jitter <= 0.1 ns.
	The local time counter should be synchronized with the time value of the central time counter by periodically distributing clock and time information via an optical TTE network.
	The TTTE system must provide time capturing functions for data acquisition purposes as well as functions for producing trigger signal sequences and clock signals.
Tigger functions	It should be possible to receive, process and output trigger signals.
Event functions	The system must be able to distribute and process of event messages.

III. TTE SYSTEM OVERVIEW

The TTE system has a hierarchical structure, as shown in Fig. 1. The central TTE (cTTE) system is at the top of this structure and is assigned to the central control system of W7-X.

The main functions of the cTTE system are provided in the cTTE device. An oven-stabilized clock generator generates the master clock with a frequency of $f = 50\,MHz$ for the central and local clocks.

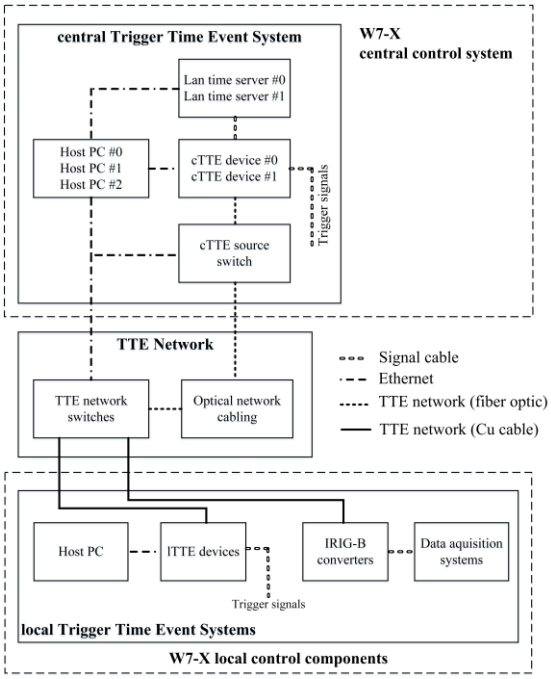

Fig. 1. Structure of W7-X TTE system.

This clock generator can be controlled by the clock of the Local Area Network (LAN) Time Server (ML600, MEINBERG Funkuhren GmbH, Germany) via a control loop.

The clock is doubled to 100 MHz in the cTTE device and drives bit 1 of a 64-bit time counter, whereby the time counter counts in 10 ns increments. The 64-bit register value of the cTTE time counter corresponds to UTC (Universal Time Coordinated).

The time counters of the Programmable Logic Controllers (PLCs) and computers with low time resolution requirements are synchronized by a connection to the LAN time server using the NTP protocol.

The cTTE device has an optical transceiver module that communicates with the local TTE (lTTE) systems via an optical unidirectional network (use of the device version cTTE Version 1: cTTE_V1) bidirectional network (use of the device version cTTE_V2). Clock and time information as well as event messages are transmitted to the local TTE systems. Once the new expansion stage of the TTE system has been commissioned, the lTTE devices can transmit event messages to the central TTE system.

The TTE network switch devices in the TTE network are responsible for dividing the TTE network into the required number of subnets and ultimately for providing the ports required for connecting the local TTE devices.

To ensure high availability, the central TTE system components – specifically, the cTTE device, the cTTE control computer, and the LAN Time Server are designed redundantly. This redundancy enhances system reliability by providing backup options in case of component failure.

The cTTE source switch device connects the transmission signal of the active cTTE_V2 device to the downlink of the TTE network. The cTTE_V2 master and slave device receive all messages from the local TTE devices via the uplink of the TTE network.

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The TTE network and the local TTE systems are designed without redundancy.

The lTTE_V2, cTTE_V2 and TTE network switch_V2 devices are connected to their assigned Host computer via a 1 GBit/s Ethernet interface to exchange configuration data, control commands, and status and timing data. The cTTE / lTTE devices of the previous version V1 were computer cards with a PCI bus interface.

For clock synchronization, the cTTE_V2 device is connected to the 1pps signal of the LAN Time Server.

The cTTE_V2 and lTTE_V2 devices have several I/O ports with special functions (such as pulse generator outputs, triggering of the time capture function and triggering of predefined event messages) and Input/Outputs (I/O) ports for user-defined functions.

IV. New Developments

The existing TTE devices were further developed based on operating experience with the TTE system and the wishes of the users. Table II shows an overview of revisions of the TTE devices.

TABLE II
OVERVIEW OF TTE DEVICE CHANGES

Development	Replacement for	Available since
lTTE_V2 device	lTTE_V1 PCI card	2022
cTTE_V2 device	lTTE_V1 PCI card	2023
cTTE signal source switch_V1	-	2024
TTE network switch_V2	TTE network switch_V1	2024
IRIG-B signal converter	-	2022

Table III provides an overview of important new or changed requirements that must be taken into account when developing version 2 TTE devices. An important basic requirement for the further development of TTE devices is that version lTTE_V1 devices can continue to be used in the TTE system.

The most important changes to the TTE devices are presented below.

A. Changes of lTTE_V2 device

The lTTE_V1 Peripheral Component Interconnect (PCI) card was the first TTE device to be converted to a 1 RU 19” device with a 1 GBit/s Ethernet interface. Fig. 2 shows the block diagram of an lTTE_V2 device.

A comprehensive description of the structure and features of the lTTE_V2 device is given in [24]. After completion of the operating phase OP2.1 in May 2023, identified deficiencies in the Field Programmable Gate Array (FPGA) program were corrected and new features were implemented for the transmit data module and for the pulse sequence generator module.

In the FPGA program, the Pulse Sequence Generator (PSG) module has been fundamentally revised to simplify the application for the user.

The PSG module uses so-called patterns, programs and sequences to generate pulse sequences.

Patterns are based on predefined bit sequences. For each pattern, the time length of a bit is defined with the value "high" and a bit with the value "low". The bit times of a logical 1 and a logical 0 are configured as multiples of the system clock TCLK.

A pattern has a maximum length of 32 bits. The number of bits/pattern used (pattern length) is defined for each pattern. A maximum of 16 different patterns can be defined.

A program consists of a sequence of max. 16 different patterns. For each pattern in a program, you can specify whether it is to be executed once or several times before the next program step is processed.

TABLE III
OVERVIEW OF NEW OR CHANGED REQUIREMENTS FOR THE TTE DEVICES VERSION V2

New or modified requirements	Motivation / Implementation
Availability of electronic components	Use of FPGA Virtex 6 (Xilinx) due to end of production of the Virtex 1000E,
Improving the power reserve for data transmission in the optical TTE network	Use of a new optical transceiver circuit (CR 155, Corretec) with higher transmission power to reduce the bit error rate during data transmission.
Changing the mechanical design of the cTTE and lTTE devices	Installation of the electronics of the cTTE_V2, lTTE_V2 and TTE network switch_V2 devices in a 1 RU 19" housing, to be independent of the housing type of the host PCs.
Improvement of I/O port cabling	Easily accessible I/O connections on the front and rear of the lTTE_V2 and cTTE_V2 devices,
Facilitate commissioning and troubleshooting	Use of an alphanumeric display to output status information and status indicators on the front of the lTTE_V2, cTTE_V2, and TTE network switch_V2 devices,
Improving the cooling of the electronics	Integration of active fans for air conditioning the electronics in the TTE devices to reduce temperature drifts of the electronics,
Modification of the interface between Host PCs and TTE devices	The use of a 1 GBit Ethernet interface for the lTTE_V2, cTTE_V2 and TTE network switch_V2 devices enables access from one PC to several lTTE_V2 devices and a separation of the installation location of the TTE_V2 devices from their host PCs
Bidirectional sending of event messages	The implementation of the transmission channel from the lTTE_V2 devices of the local TTE systems via the TTE-Switch_V2 devices to the cTTE_V2 device enables event messages to be sent, received and processed in both the central and local TTE systems
Bug fixing of FPGA software	Correction of detected errors in the FPGA programs of the lTTE_V1 and cTTE_V1 devices,
Enhancement of the functionality of the lTTE_V1 and cTTE_V1 devices	Use of the DDR3 memory newly inserted for the lTTE_V2 device for the storing the time values of the Time Capture_FIFO device, Insertion of the modified Pulse Sequence Generator module for the lTTE_V2 devices,

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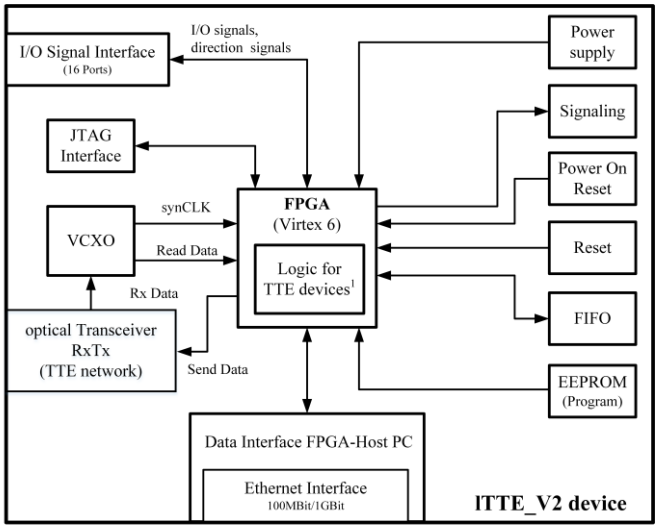

[1]**TTE devices:**
time counter (1x), time capture (8x), pulse generator (2x), pulse sequence generator (1x), delay timer / counter (8x), alarm timer (2x), I/O devices (16x), device map matrix (1x),

VCXO:
Voltage Controlled Crystal Oscillator,
FIFO:
First In- First Out (buffer),

Fig. 2. Block diagram of lTT_V2 device.

When a sequence program is started, programs are processed in a defined order. Each sequence program has a maximum of 16 steps. The program to be executed is defined for each step.

A maximum of 16 different sequence programs can be defined. It must be specified whether a sequence is to be processed once or several times. It is possible to define an endless loop for the continuous repetition of the sequence. First, patterns are defined from bit sequences (patterns), which can contain a maximum of 128 bits. The bit length of 0 and 1 is simply defined by a configuration parameter for each pattern individually. Fig. 3 shows the configuration process for a pulse sequence.

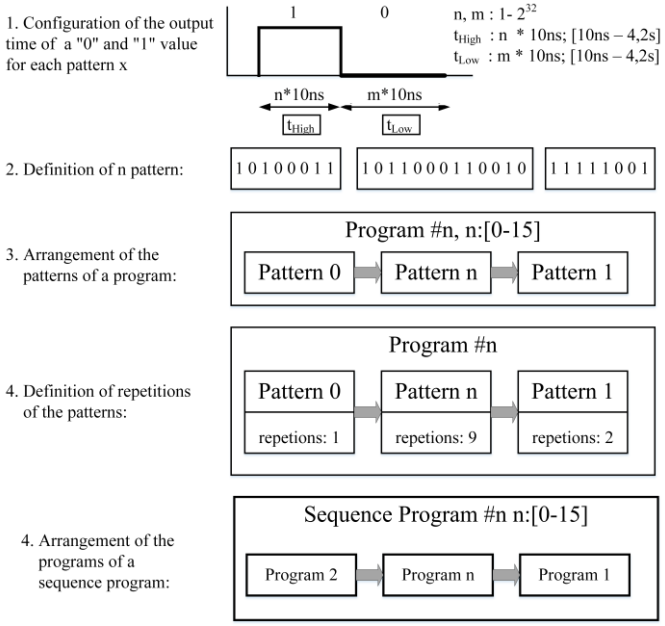

Fig. 3. Programming scheme of the new PSG module of lTTE_V2 device.

B. *lTTE_V2 Device for Standard Trigger Application*

A lTTE_V2 device with a special FPGA configuration was programmed for easy integration of data acquisition into the W7-X experiment sequence.

In this FPGA configuration, the event message module and 7 I/O trigger modules were statically configured so that an assigned trigger generates an output signal when a specific event message is received. The individual triggers are linked to the start time of different experiment phases (see Fig. 4). The event messages are sent by the cTTE_V2 device at the instigation of the central experiment sequence controller.

By using the standard trigger, the diagnostic system can decide which activities it wants to start or end for which trigger.

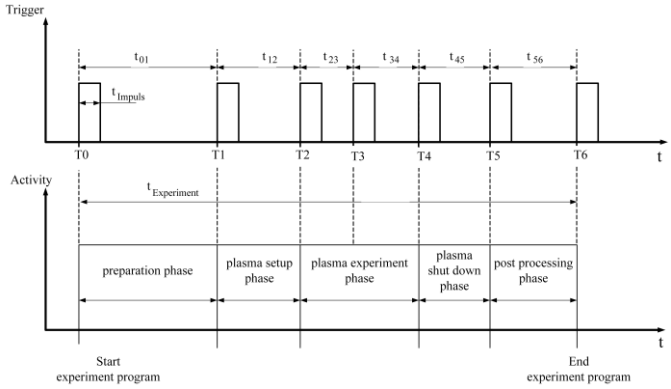

Fig. 4. Standard Trigger sequence for a plasma experiment program.

C. *The cTTE_V2 Device*

The functions of the previous cTTE_V1 PCI card have been implemented in a 1 RU 19” device with a 1 GBit Ethernet interface to its control PC. The functional structure of the cTTE_V2 device is shown in the block diagram in Fig. 5.

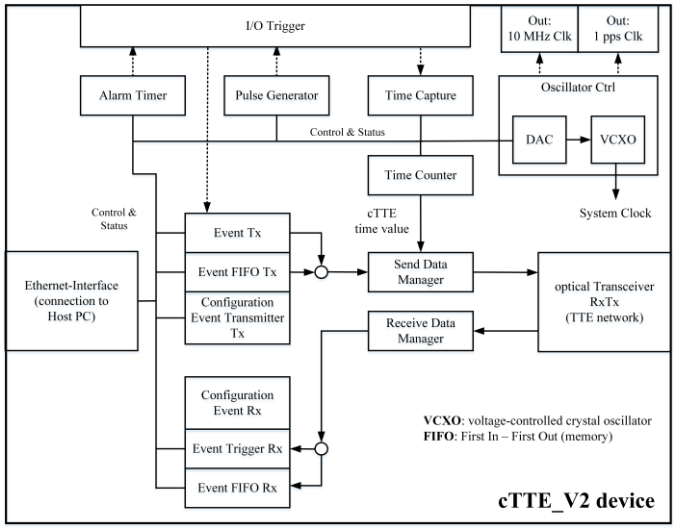

Fig. 5. Block diagram of a cTTE_V2 device.

Fig. 6 shows a front view of the cTTE_V2 device. The internal hardware structure of the cTTE_V2 device is shown in Fig. 7.

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Fig. 6. Front view of cTTE_V2 device.

This device uses the same FPGA board (4) as the lTTE_V2 device, which has significantly reduced the development effort. This FPGA card is equipped with a Virtex 6-130t FPGA and a DDR3 RAM module. The motherboard (3) with the power supply unit (1), signal driver, and oven stabilized oscillator board (2) are new developments.

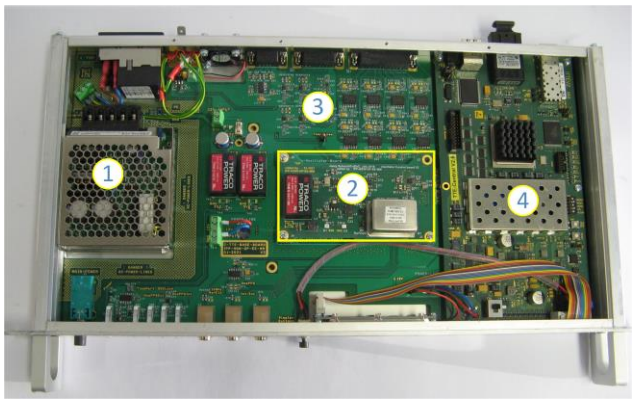

Fig. 7. cTTE_V2 device with open housing.

D. The TTE Network Switch_V2 Device

TTE network switches have the task of connecting the central TTE device with any number of local TTE devices via an optical network. Synchronization information, time data packets and event messages are exchanged via this network. The TTE network switches_V2 devices have one uplink port and 8 downlink ports.

Version V1 of the TTE network switch device was based on electronics without an FPGA and was designed only for a unidirectional optical connection from the central TTE to the local TTE devices.

For the operating phase OP2.1, version V2 of the TTE switch was developed to meet the requirements of new lTTE_V2 and cTTE_V2 devices. Fig. 8 shows the functional structure of the TTE network switch_V2 device.

The FPGA card of the TTE network switch_V2 is identical in hardware design to the lTTE_V2 card, and supplements the basic functions of the TTE network switch_V1 device by adding the reverse transmission direction and its transmission prioritization.

Fig. 9 shows a TTE network switch_V2 device with its 8 optical downlink ports. There is a fiber optic connection on the back, which represents the uplink (UL). The UL is used to connect the switch to the next higher hierarchy level, which can be either another TTE network switch or a cTTE device.

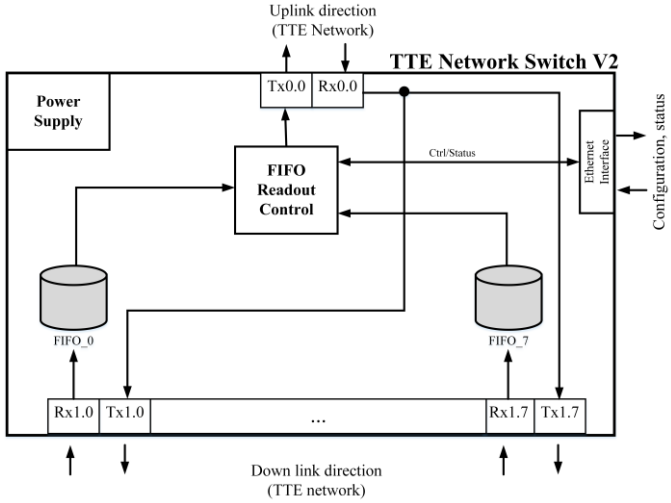

Fig. 8. Block diagram of TTE network switch_V2 device.

Fig. 9. Front view of a 19" TTE network switch_V2 device.

Inside the switch is an FPGA that takes over the control tasks. Incoming messages at the UL are forwarded without delay to all outgoing DL ports. The core function is the intermediate storage of incoming time and event messages from the fiber optic network in FIFO structures and their sequential forwarding to the outgoing UL port.

The TTE network switch_V2 device has two basic operating modes for message transmission: standard mode and priority mode. The standard mode is the default mode, which is used directly after the switch is started and without any configuration. In standard mode, the incoming data from the receivers of the DL ports is temporarily stored in FIFO structures before this data is sent to the next higher level of the fiber optic network via the transmitter of the UL port. By using a round-robin scheduling method, the FIFOs are read in ascending order. If there is a message in the respective FIFO, it is sent and the logic moves on to the FIFO with the next higher number. After FIFO 7, the logic starts again at FIFO 0.

In the priority mode, each FIFO is assigned a priority by the user. The control register responsible for this is written via Ethernet using a configuration message. The FIFO with the highest priority is read out completely first before switching to the FIFO with the next priority. If data is received on ports with a higher priority while a FIFO with a lower priority is being read and the entry is currently sent out, all existing, higher priority FIFO entries are processed according to their configured priority once the current transmission process has been completed. The standard prioritization is according to the port numbers from 0 (highest priority) to 7 (lowest priority) which can be changed in the configuration registers.

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Fig. 10 shows an example procedure with only two occupied ports. Event message data from Port 1.0 have a higher send priority than data from Port 1.1. The messages displayed at receivers (RX) and transmitters (TX) are the sequential incoming and outgoing serial data of the respective optical ports. Once a message has been received in full, its content is temporarily stored in a FIFO. The Uplink REG represents the register for the current message to be sent. This register is written to by the priority control with the event message data from the FIFO of a corresponding port. The respective event message is then output bit by bit to the FBO uplink transmitter.

As there are no further messages in port 1 FIFO 1 at time 7, the content of port 1.1 FIFO 2 is output first. In the meantime, port 1.0 receives further messages, which are now preferentially output. Only then are the remaining event messages from port 1.1 sent out.

To determine the delay of a TTE network path in the TTE system, the switch can be set to delay measurement mode. This does not change anything on the downlink, as all data will be already forwarded directly and in parallel to all T1.x port transmitters.

The uplink port P1.x to be activated for the delay measurement is configured via Ethernet. The data received at the receiver R1.x of the configured port P1.x is direct forwarded to the uplink transmitter T0.0.

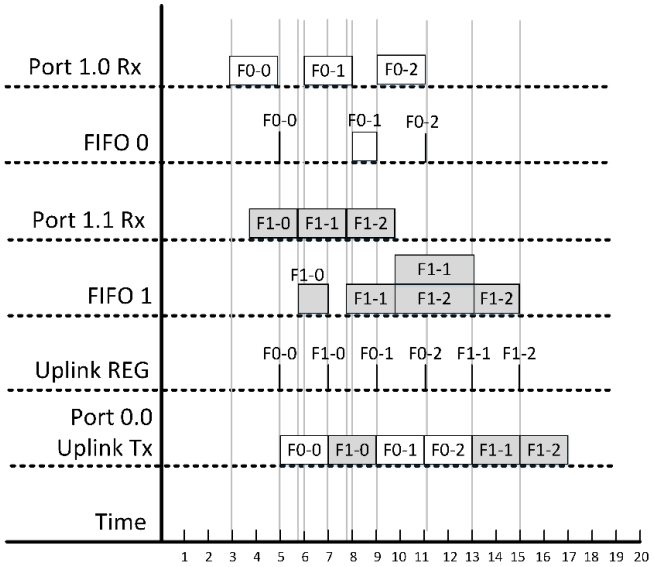

Fig. 10. Message processing in a TTE network switch_V2.

The last TTE network switch in the TTE network hierarchy, which connects the lowest level lTTE devices, is a special case. To measure the transmission delay in a TTE network section, the data to be sent via the T1.x transmitter of port 1.x of a TTE network switch is mirrored directly to the Tx0.0 data transmitter of the uplink port through of a configured short circuit. This means that the received data packet can be sent directly back to the cTTE_V2 receiver. The transmission time of the measurement data for the selected network route can then be determined in the cTTE_V2 device and the delay is calculated from this.

An activity diagram for the delay measurement processing in TTE network is shown in Fig. 11.

E. The TTE Signal Source Switch Device

The TTE signal source switch_V1 device is a new development. When operating the two cTTE_V2 devices in redundant mode, the transmission signal of the active cTTE_V2 device must be transmitted to the local TTE system via the TTE network. The TTE signal source switch_V0 device is responsible for switching the transmit signal. It is equipped with a µController (µC) board with an Ethernet interface. The signal source can either be switched manually or remotely. Fig. 12 shows a block diagram of the functions of the TTE signal switch device.

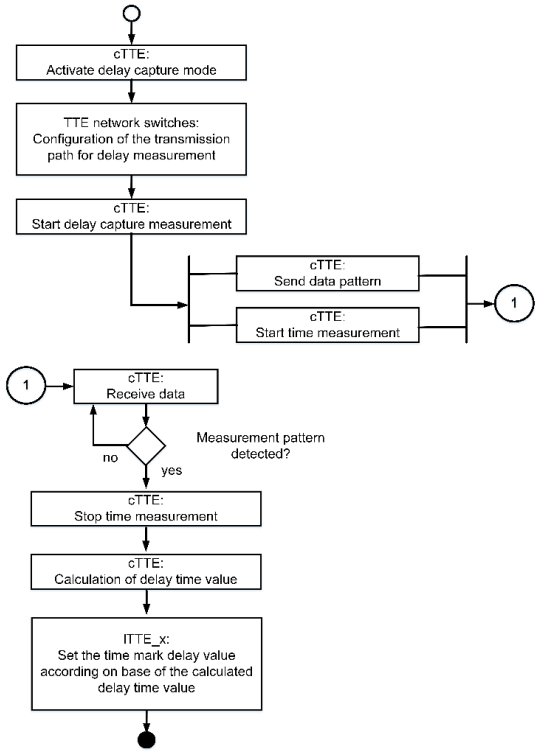

Fig. 11. Activity diagram for the delay measurement of a TTE network path.

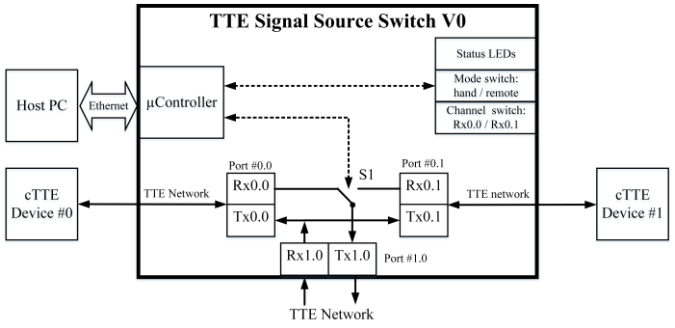

Fig. 12. Block diagram of TTE signal source switch_V0 device.

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F. The IRIG-B Converter Device

Products from Gantner Instruments [11] are often used at W7-X to measure mechanical and thermal variables. These measurement modules can be synchronized via the IRIG-B protocol. A converter module has been developed so that these Gantner measuring systems can be synchronized to the W7-X time of the cTTE system. It has a connection to the TTE network and receives the periodic time information from the cTTE system. The IRIG-B (Inter Range Instrumentation Group Timecode B) coded time signal is then output to the measuring modules.

The converter module is based on a commercial FPGA AMD Spartan 6 baseboard module TE0600 (company trenz electronic) and an electronic board for the optical receiver of the TTE network signal and output of the electrical IRIG-B signal. A block diagram of an IRIG-B converter is shown in Fig. 13. The IRIG-B converter has a top-hat rail housing, as shown in Fig. 14.

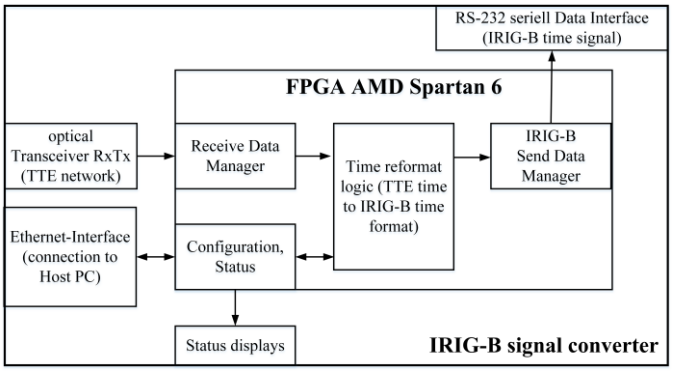

Fig. 13. Block diagram of IRIG-B converter device.

Fig. 14. IRIG-B converter device.

V. TESTS

The functional tests of the TTE devices of type lTTE_V2, cTTE_V2 and TTE network switch_V2, and the cTTE signal source switch_V1 were successfully completed. Due to the high complexity of the cTTE_V2 and lTTE_V2 devices in particular, the test scenarios had to be carefully selected and carried out.

The following characteristic values were determined for the oscillator modules of the cTTE_V2 and lTTE_V2 devices:

A. Oscillator cTTE_V2 Device

- Circuit: Quartz oscillator Quintenz QO27366SC,
- Type: Oven-stabilized voltage-controlled oscillator,
- Application: Voltage controlled oscillator in a proportional-integral-differential (PID) controller for synchronization of the oscillator clock CLK with the reference clock of a LAN time server,
- Frequency: f_0=10MHz ± 0,3ppb,
- Frequency stability: ± 0,5ppb (ppb: parts per billon),
- Reference Tuning Range: ±2ppm (Δf= ±20Hz),
- Control voltage: 0-4V, produced by a 18 Bit DAC (Digital-to-Analog) converter Texas Instruments TI8981,

B. Oscillator lTTE_V2 Device

- Circuit: Quartz oscillator VECTRON TRU155,
- Type: Varactor tuned crystal oscillator,
- Application: Phased locked loop (PLL) for clock recovery of TTE network data stream,
- Frequency: f_0=50MHz ± 75ppb,
- Frequency stability: ± 75ppm (ppm: parts per million),
- Reference Tuning Range: ±50ppm (Δf= ±2.5kHz),
- Control voltage: 0-4.5V,

C. Transmission Delay Measurement

The cTTE_V2 devices are equipped with a module for measuring the transmission times on the TTE network. This measurement is usually carried out when setting up a new transmission path. The measured delay value depends on the length of the optical path and the number of integrated TTE network switch devices.

During this transmission delay measurement, the transmitter Tx of the cTTE_V2 device sends out a special data pattern in the network path under consideration. This data pattern is immediately sent back to the cTTE_V2 receiver Rx by the last TTE network switch_V2 device. The time between sending and receiving the pattern is measured. The measured transmission time is divided by 2 and this value can then be entered in a special configuration register on the lTTE_V2 device. The delay between the last TTE network switch and the lTTE_V2 device can usually be ignored or must be added manually to the delay value. This delay value allows a greater accuracy when synchronizing the time value of the lTTE_V2 time counter device with the central time of the cTTE system.

Tests with 4 well known lengths of optical network cable (100m, 200m, 300m, and 400m) have confirmed that the delay measurement enables a time resolution of 4ns.

D. TTE System Test Bed

A comprehensive test bed for the entire TTE system is currently being set up. For this purpose, a complete TTE system with a redundant central TTE system, three TTE network switch devices_V2 and three local lTTE_V2 devices are being set up in an electrical cabinet. The length of the network cables for the TTE network can be varied. The TTE test system is a permanent setup that will be used to test both the individual TTE devices and the overall TTE system.

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VI. Status and Outlook

New versions of the lTTE device and the cTTE device have been developed for the future-proof operation of the TTE system. The lTTE_V2 devices were in use since the OP1.2b operating phase. However, the FPGA configuration of these devices has been partially revised. The new devices for the central TTE system (cTTE_V2 devices, TTE network switch_V2, TTE signal source switch_V1) are not yet being used for the upcoming OP2.2 phase, as they still need to be extensively tested together with the new application software. A comprehensive test system is currently being set up for this purpose, which contains all the necessary central and local components of the TTE system.

The number of lTTE_V2 devices still available is limited. It must therefore be decided soon whether a new FPGA card with a new FPGA type must be developed to meet the future demand for lTTE_V2 devices.

Another ongoing working package is the development of a joint FPGA software for both lTTE_V2 and cTTE_V2 devices.

Furthermore, the previous static determination of transmission delays in the TTE network is to be replaced by dynamic measurement of the delays.

VII. Summary

In summary, this article has outlined the recent developments and ongoing initiatives within the TTE system for the W7-X fusion experiment. Key advancements include the introduction of new TTE device versions, the potential development of a new FPGA card to address device availability concerns, and the ongoing effort to unify FPGA software for improved efficiency.

Additionally, plans are underway to transition from static to dynamic measurement of transmission delays in the TTE network. These efforts collectively aim to ensure the continued effectiveness and future-proofing of the TTE system to meet the evolving needs of the W7-X experiment.

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